

FH8A UMA (15.6") Haswell-H Platform Block Diagram

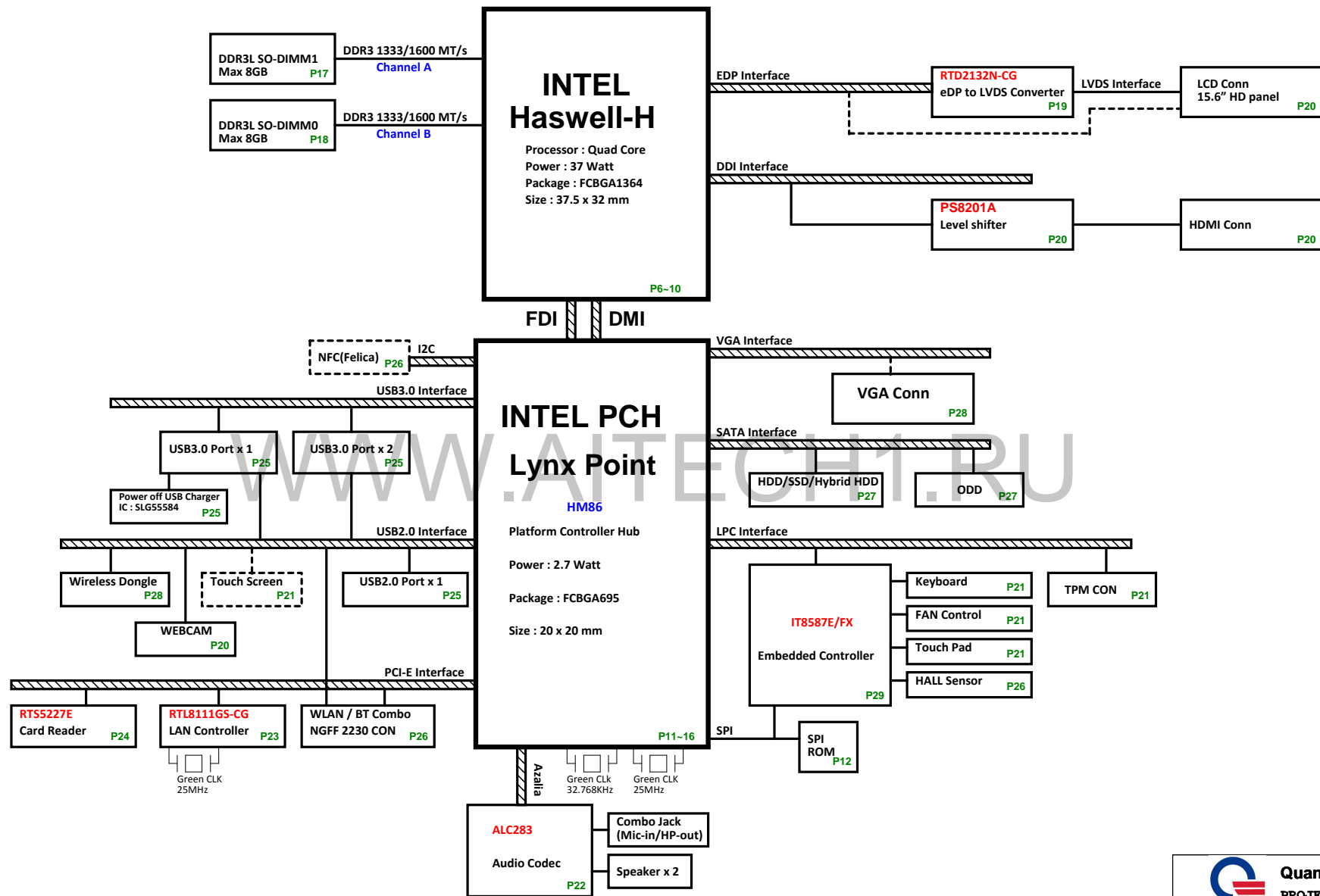


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Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	S5_ON
1.35V_S3	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
3VDUAL_LAN	3.3V	ON	OFF	OFF	OFF	OFF	LAN_ON_EC
3V_WLAN	3.3V	ON	ON	ON	ON	OFF	S5_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_2
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
1.05V_VCCST	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
DDR_VTERM	0.675V	ON	OFF	OFF	OFF	OFF	S0_ON_1
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

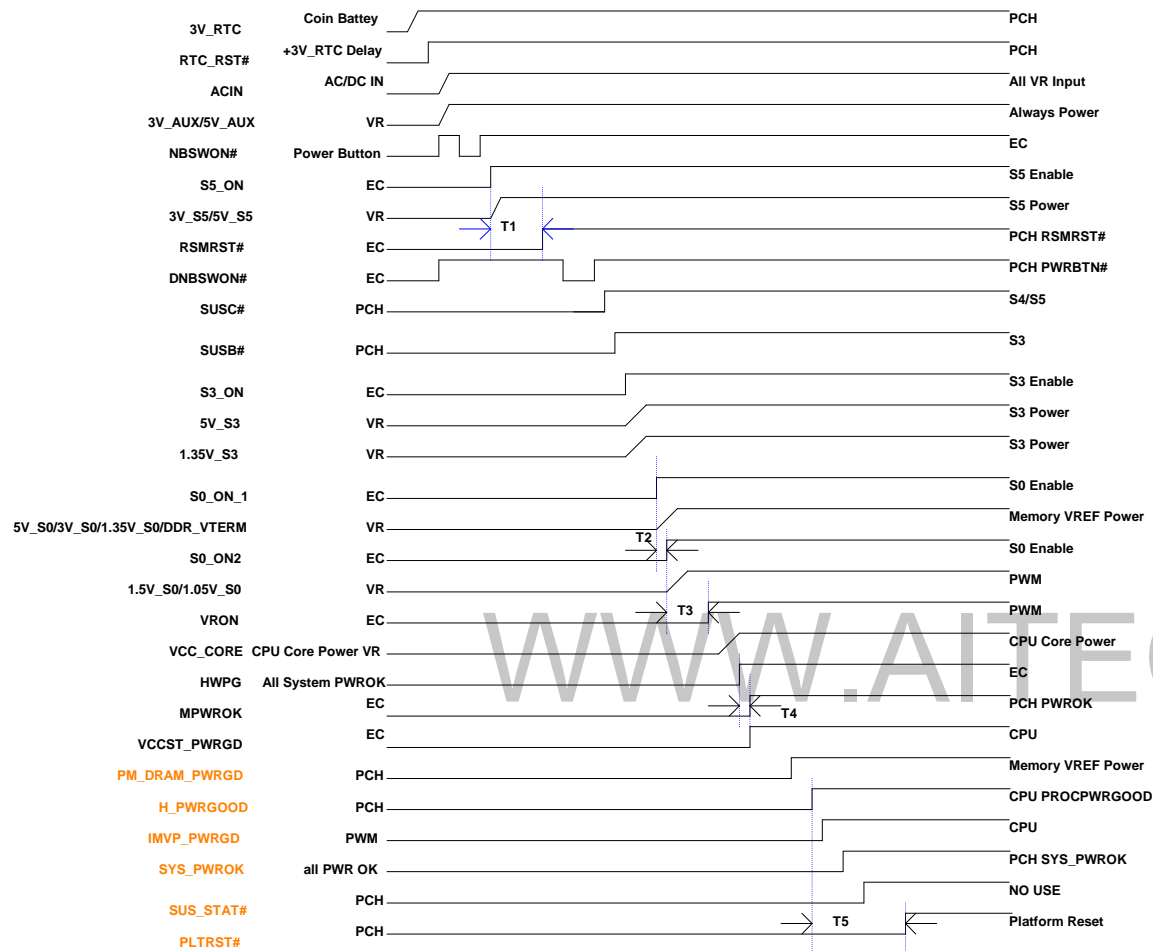
Function list

USB2		PCIE		Display		USB3		SATA	
Port 0	Co-lay USB3.0	Port 1	USB3.0 Conn	Port A	LVDS or eDP	Port 1	USB3.0 Conn	Port 0	NC
Port 1	Co-lay USB3.0	Port 2	NC	Port B	HDMI	Port 2	USB3.0 Conn	Port 1	NC
Port 2	Co-lay USB3.0	Port 3	GLAN	Port C	NC	Port 3	USB3.0 Conn	Port 2	NC
Port 3	Wireless Dongle	Port 4	NC	Port D	NC	Port 4	NC	Port 3	NC
Port 4	NC	Port 5	Card Reader			Port 5	NC	Port 4	HDD
Port 5	NC	Port 6	WLAN			Port 6	NC	Port 5	ODD
Port 6	NC	Port 7							
Port 7	NC	Port 8							
Port 8	Blue Tooth								
Port 9	USB2.0 Conn								
Port 10	NC								
Port 11	Camera								
Port 12	Touch screen								
Port 13	NC								

Function Select

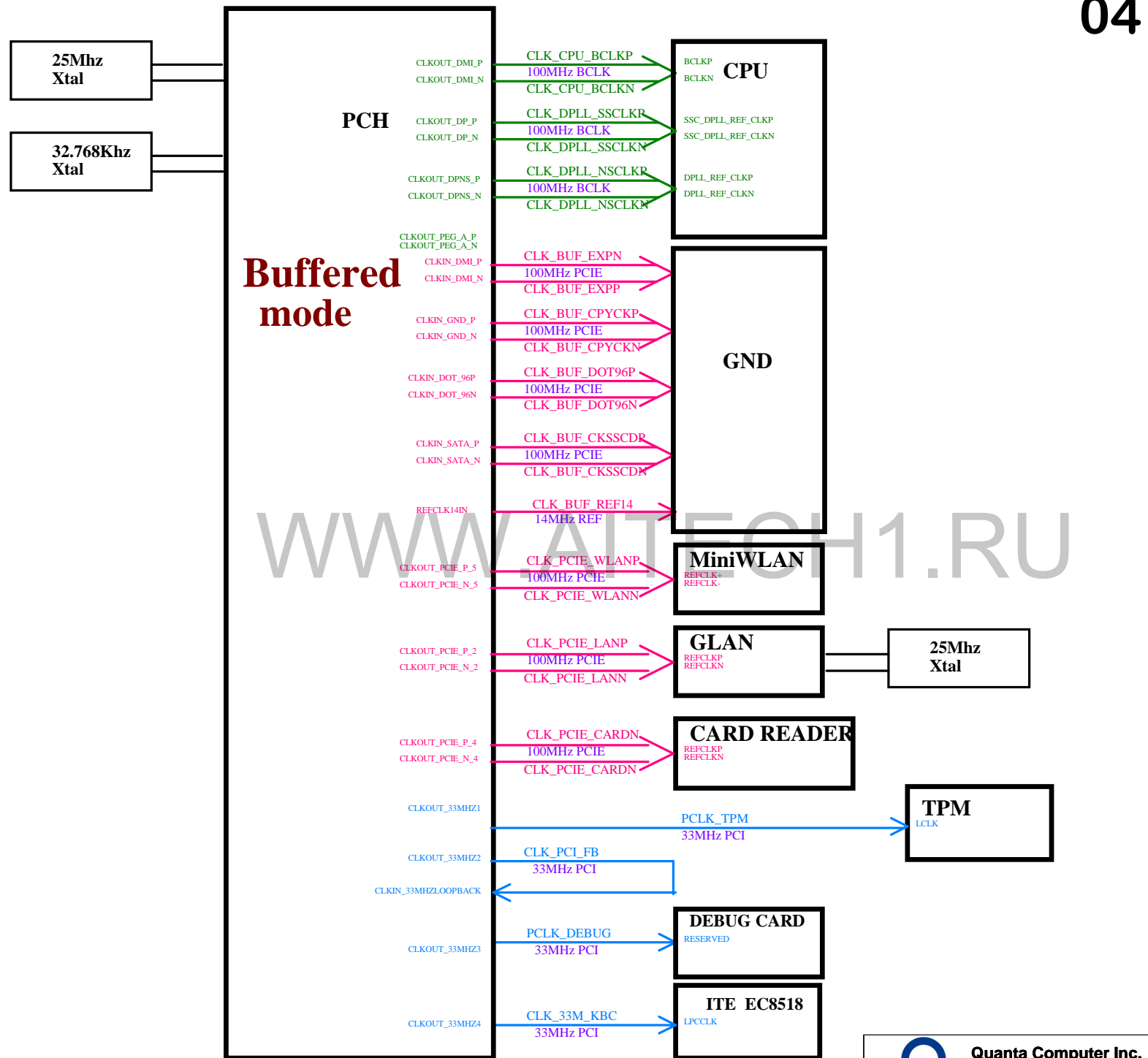
N@	NFC
L@	RTD2132N-CG
E@	Internal eDP
M@	MMB
TS@	Touch screen
C@	CRT

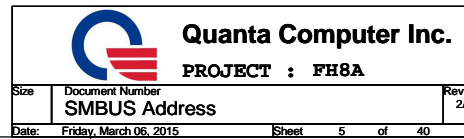
FH8A SYSTEM POWER-ON SEQUENCE



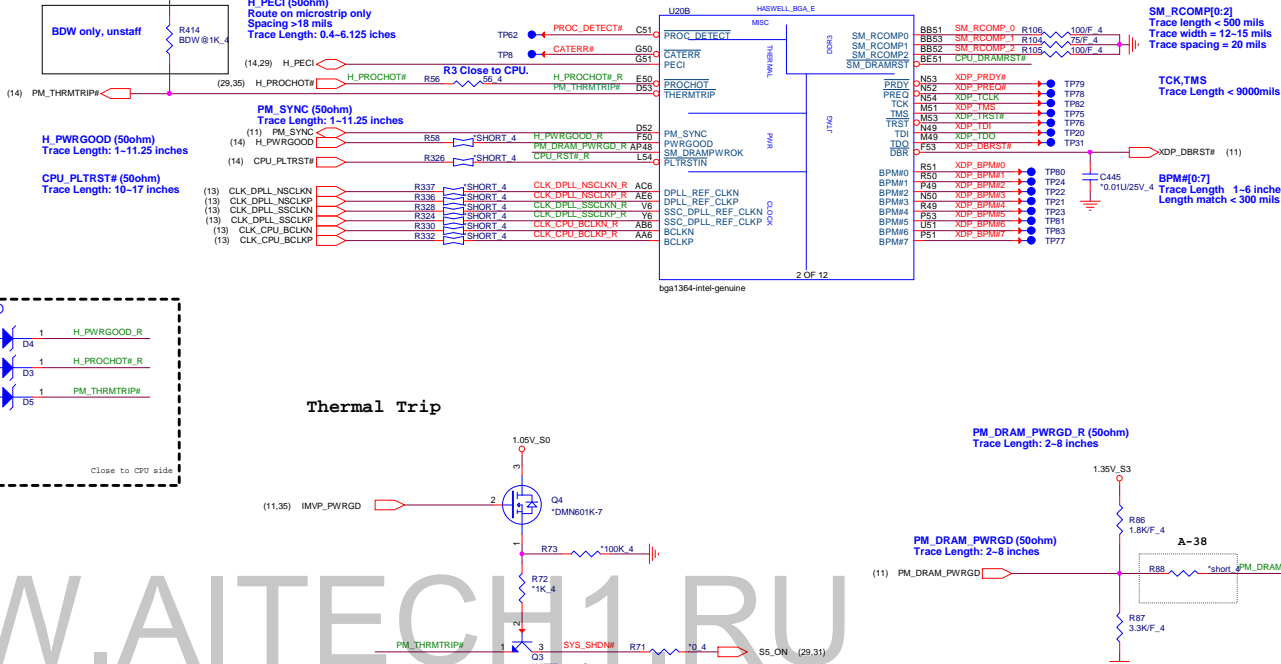
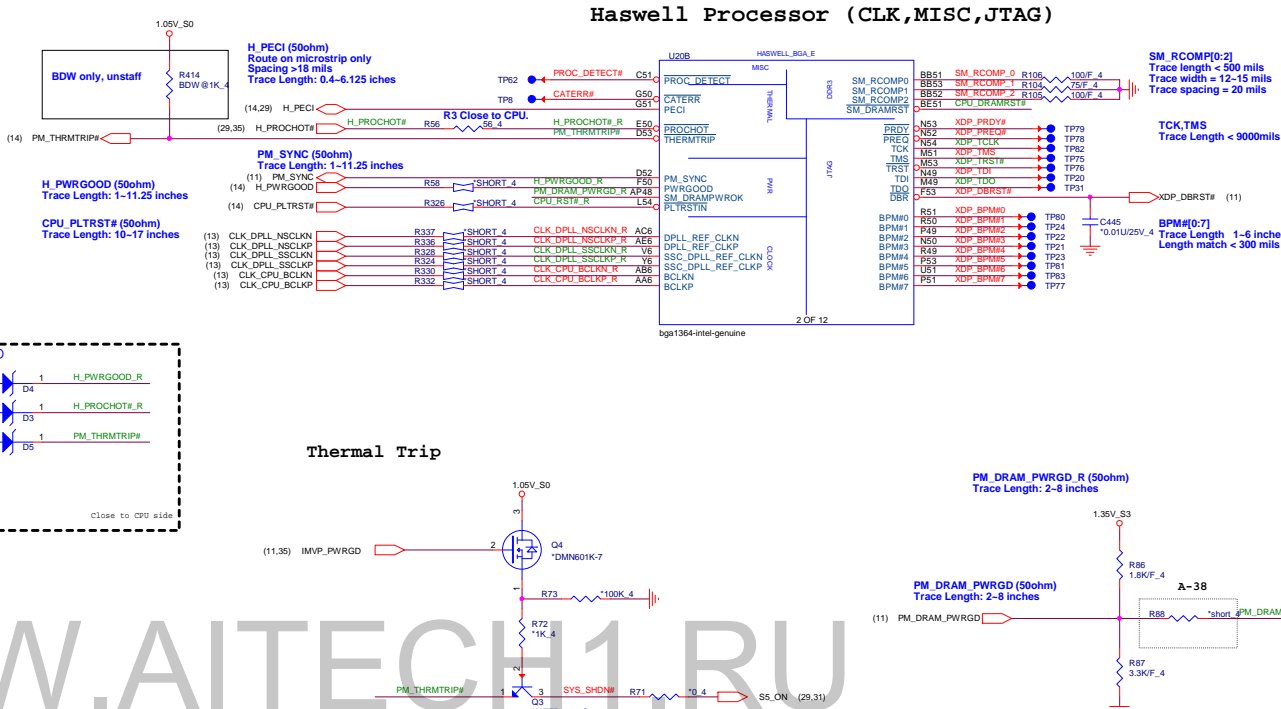
System Power Sequence

- T1: S5_ON TO RSMRST# = 20ms (spec: mini 10ms)
- T2: S0_ON1 TO S0_ON2 = 500us
- T3: S0_ON2 TO VRON = 10ms
- T4: HWPG TO MPWROK = 110ms (spec : >5~ 99ms)
- T5 : H_CPUPWRGD to PLTRST# >1ms
- T6 : VCC_CORE stable to H_PWRGOOD 5~650ms





LIGGA HASWELL, BGA, E



The schematic diagram illustrates the VCCIO_OUT pin connections for the HPS. It is divided into two sections. The top section shows two input pins: H_PROCHOT# and H_PWRRGOOD_R. H_PROCHOT# is connected to a 10K 4 resistor (R315), and H_PWRRGOOD_R is connected to a 10K 4 resistor (R57). Both resistors are connected to the VCCIO_OUT pin. The bottom section shows two input pins: CLK_DPLL_SSCLKP_R and CLK_DPLL_SSCLKN_R. CLK_DPLL_SSCLKP_R is connected to a 10K 4 resistor (R323). CLK_DPLL_SSCLKN_R is connected to two 10K 4 resistors (R531 and R327), which are then connected to the VCCIO_OUT pin. All connections are shown with ground symbols.

[illegible]

DDR3_DRAMRST# (50ohm)
Trace Length < 6 inches

Haswell ULT DRAMRST#

1.35k 53

R180
470F_4

A-27

1.75k

CPU_DRAMRST#

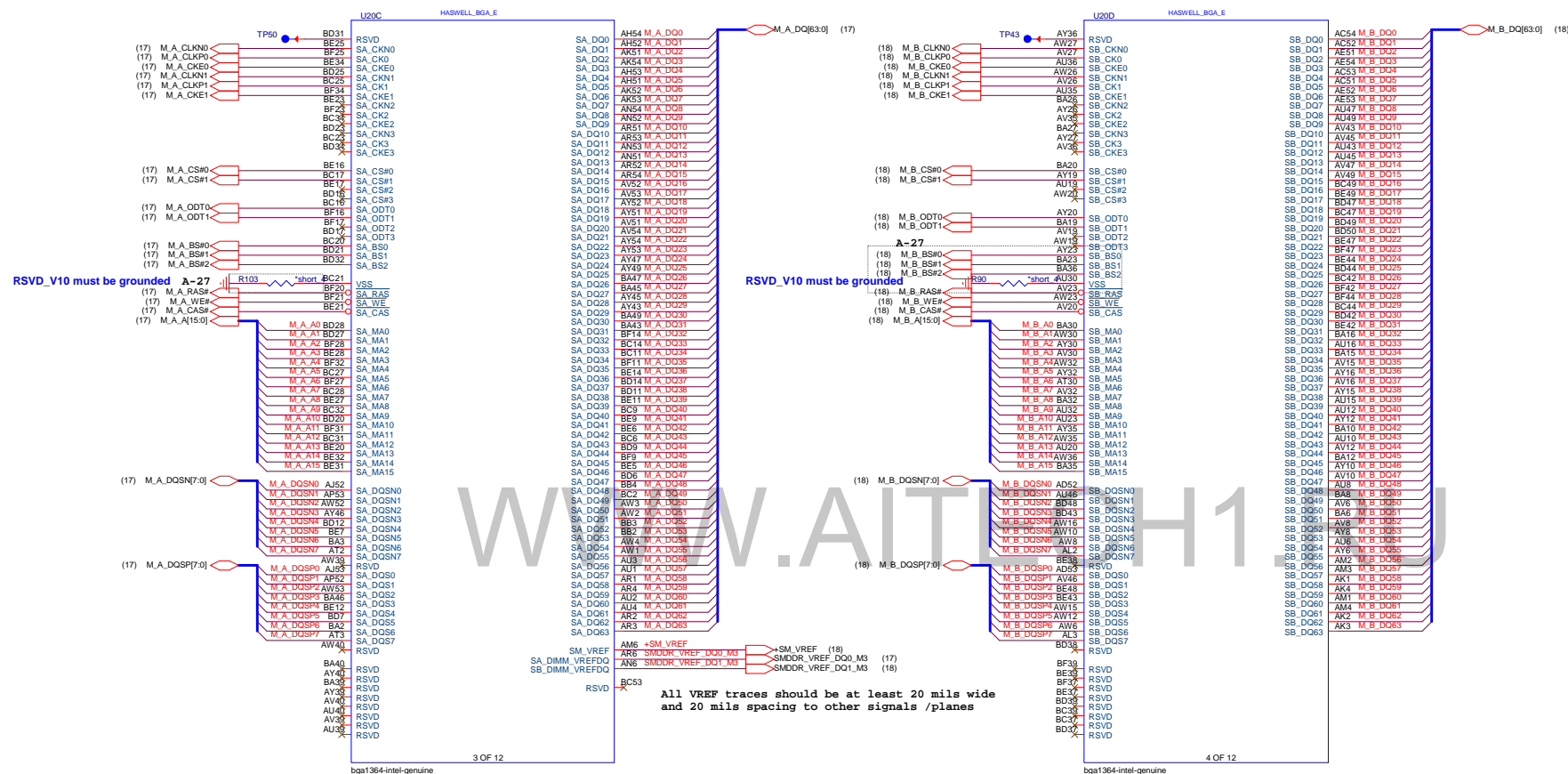
DDR3_DRAMRST#

DDR3_DRAMRST# (17, 18)

C241 0.1U16V/XTR_4

Schematic diagram showing the connection of XDP_TCLK and XDP_TRST# signals. XDP_TCLK is connected to R338 and 51_4. XDP_TRST# is connected to R335 and 51_4. Both signals are connected to a common node labeled 51_4, which is then connected to ground. A 1.05V_S0 supply is connected to R406, which is connected to *51_4, which is then connected to XDP_TDO.

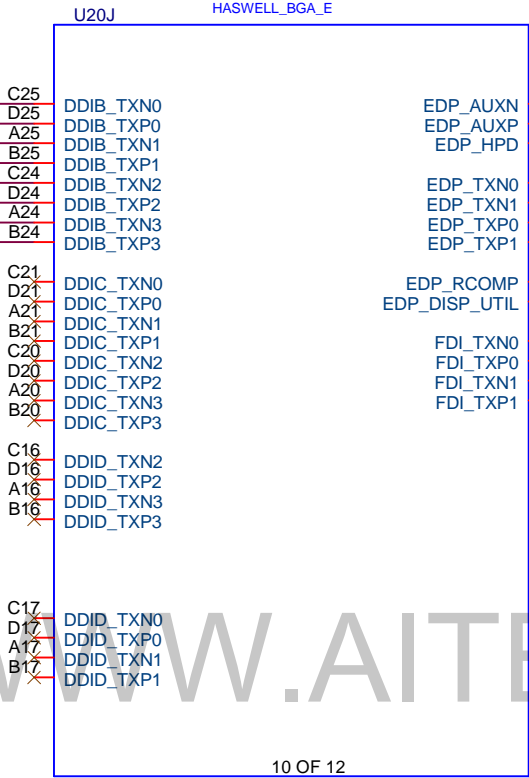
Haswell Processor (DDR3)



Haswell Processor (DDI,eDP,FDI)

HDMI

- (20) INT_HDMI_TXDN2
- (20) INT_HDMI_TXDP2
- (20) INT_HDMI_TXDN1
- (20) INT_HDMI_TXDP1
- (20) INT_HDMI_TXDN0
- (20) INT_HDMI_TXDP0
- (20) INT_HDMI_TXCN
- (20) INT_HDMI_TXCP

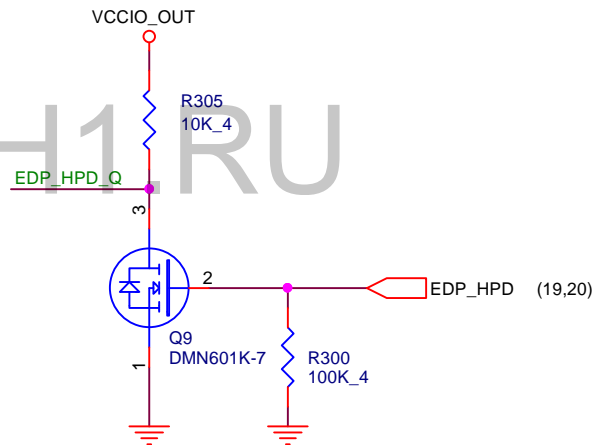


bga1364-intel-genuine

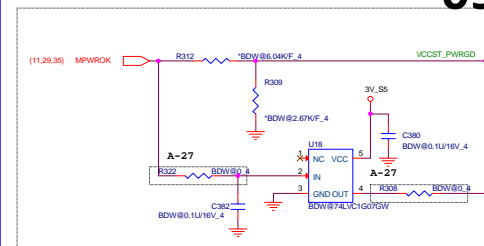
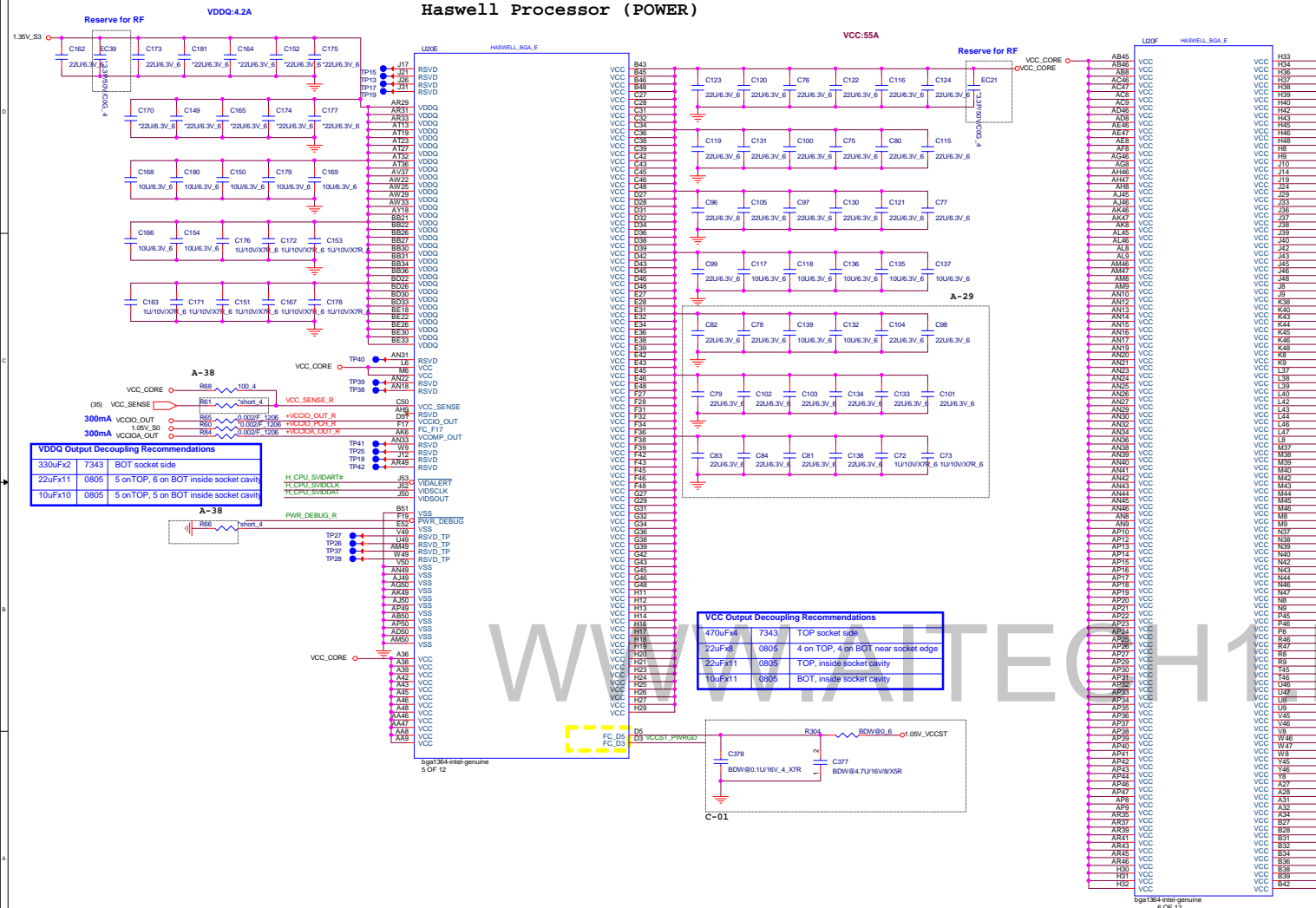
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- EDP_AUXN F15
- EDP_AUXP F14
- EDP_HPDP E14
- EDP_TXN0 C14
- EDP_TXN1 A12
- EDP_TXP0 D14
- EDP_TXP1 B12
- EDP_RCOMP AG6
- EDP_DISP_UTIL E12
- FDI_TXN0 C12
- FDI_TXP0 D12
- FDI_TXN1 A14
- FDI_TXP1 B14

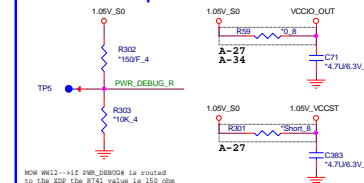
eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils



Haswell Processor (POWER)



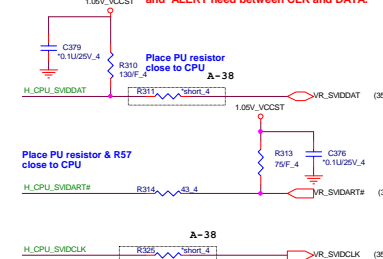
Power Test Propose



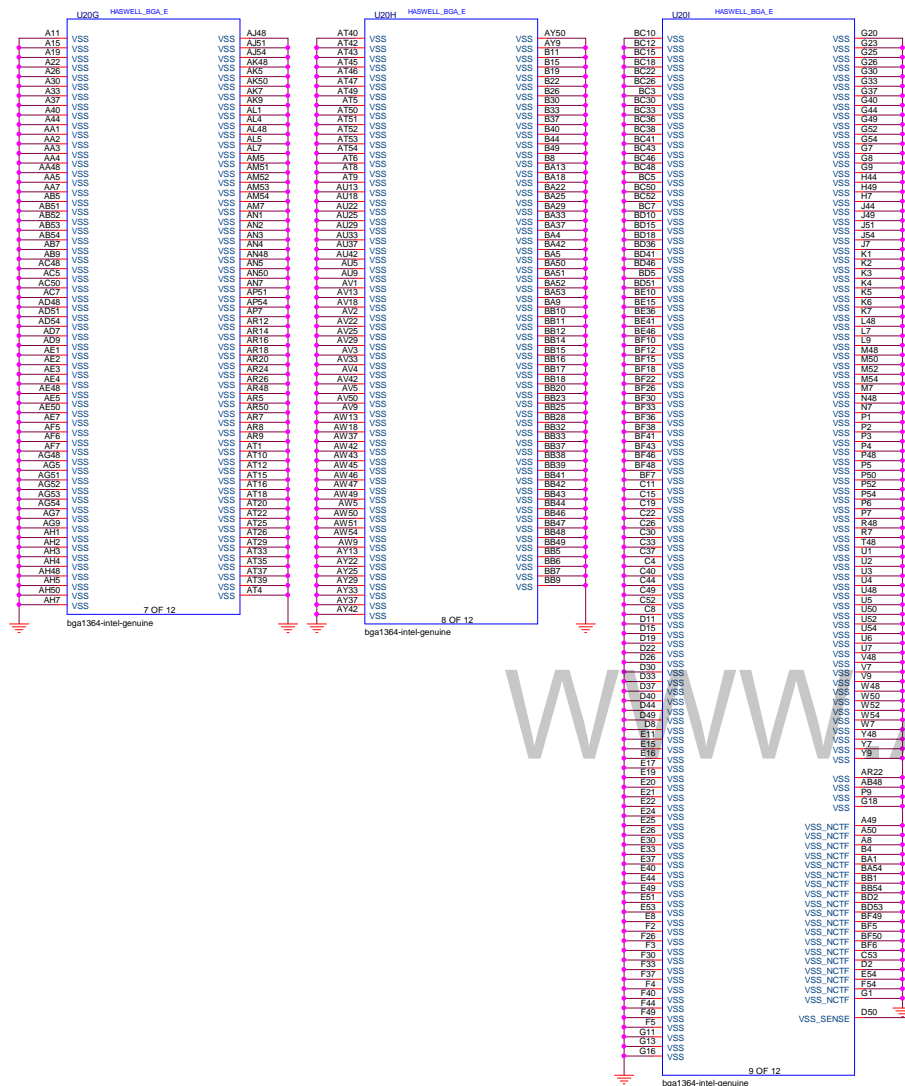
MON WW12-->if DMR_DEBUG# is routed
to the YDR the R741 value is 150 ohms

SVID

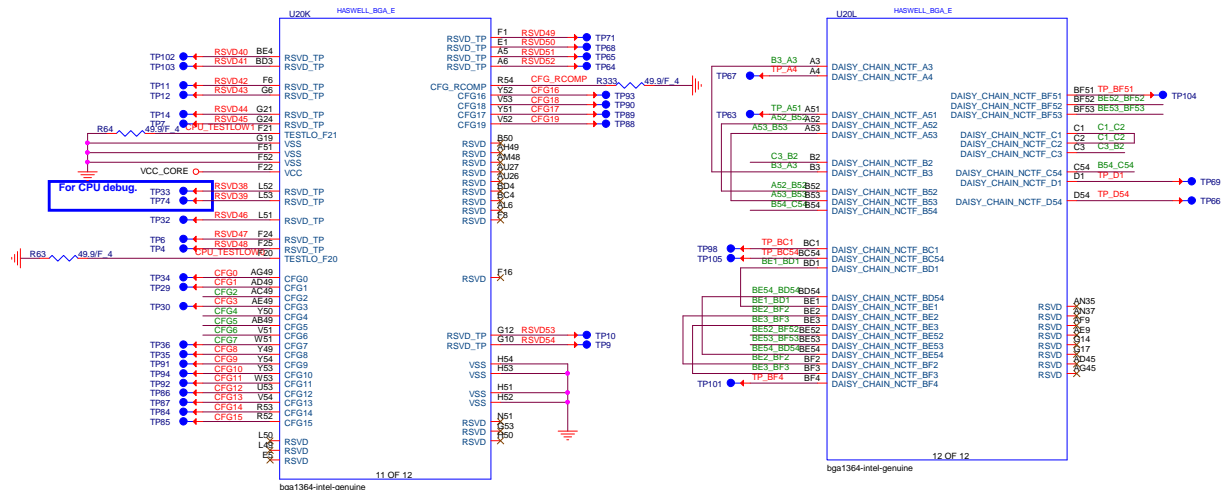
Layout note: need routing together and ALERT need between CLK and DATA.



Haswell Processor (GND)

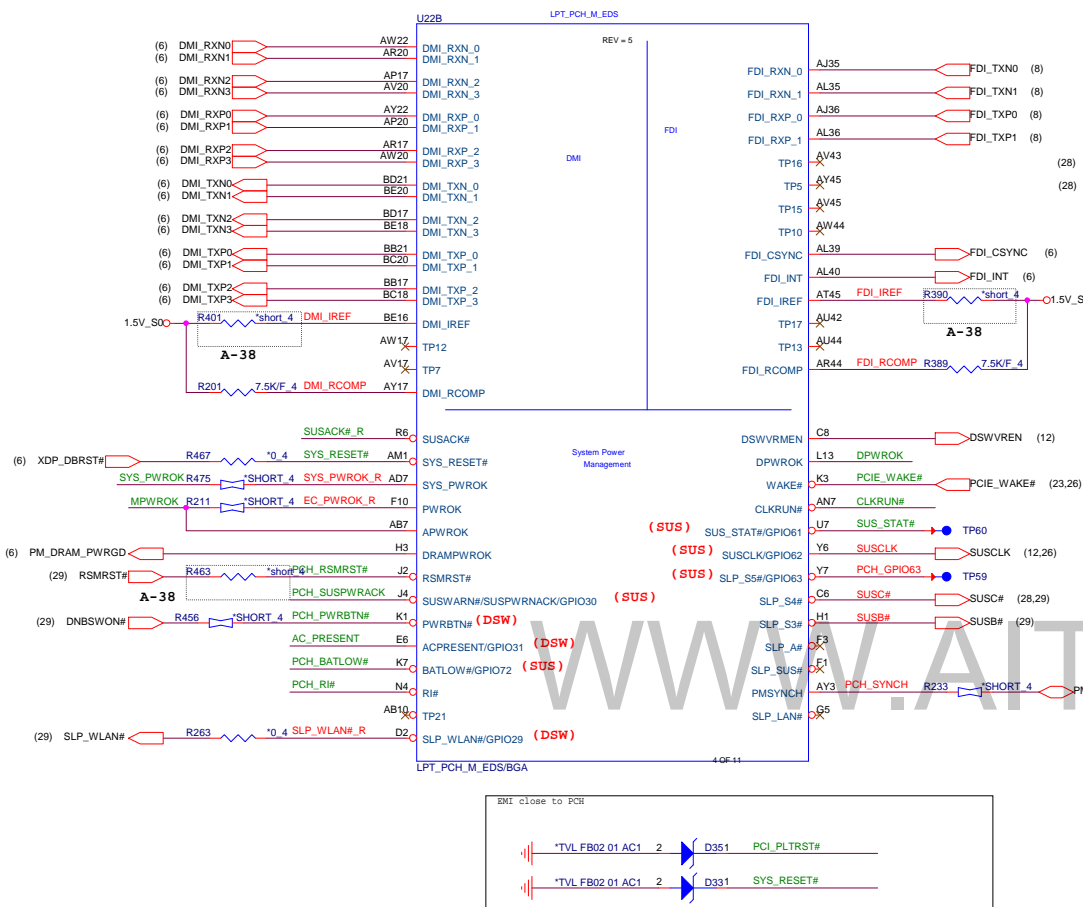


Haswell Processor (CFG,RSVD)

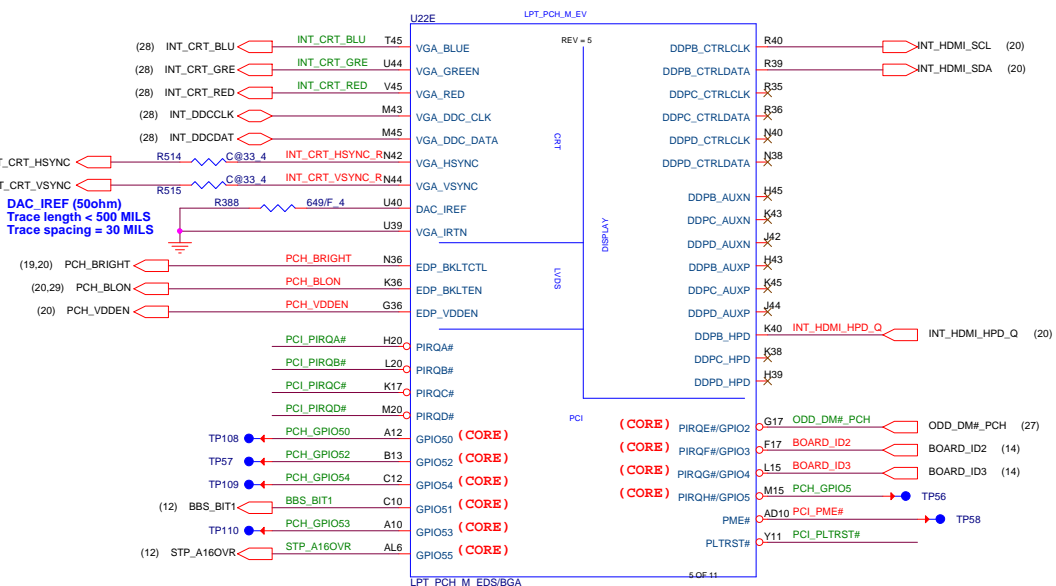


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	xDP enable	x1 = Disabled x0 = Enabled x00 = 1 x8 & 2 x4 PCI Express x01 = reserved	
CFG[6:5]	PCI Express Bifurcation	x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS for training	

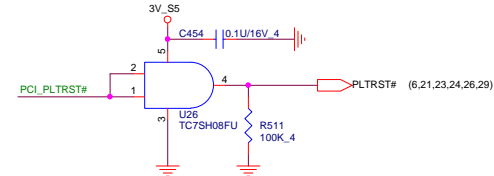
Lynx Point (DMI,FDI,PM)



Lynx Point (CRT,PCI,DDI CNTL)



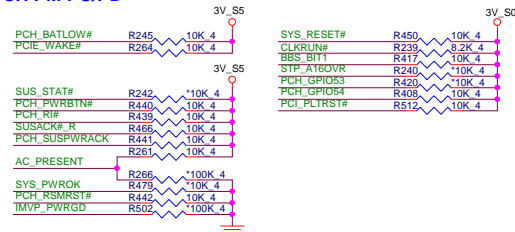
PLTRST# Buffer



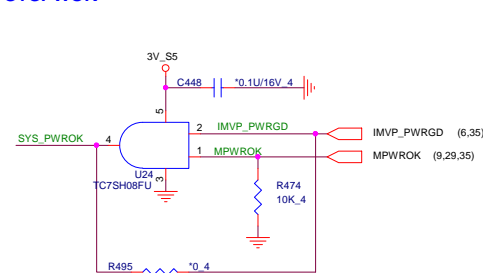
VGA PD



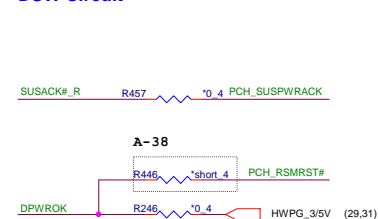
PCH PM PU/PD



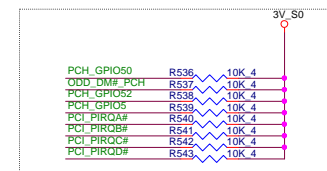
SYSPWOK



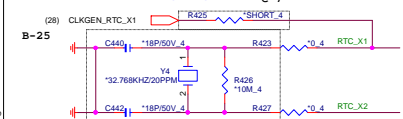
DSW Circuit



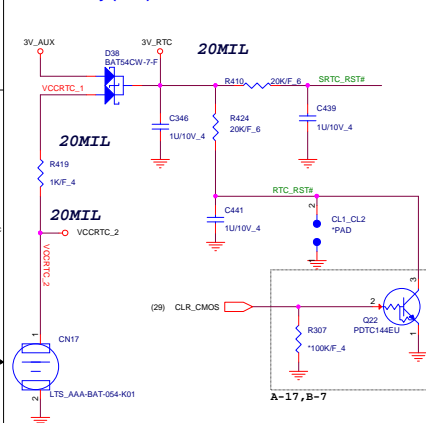
PCI PU



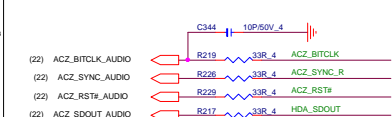
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)

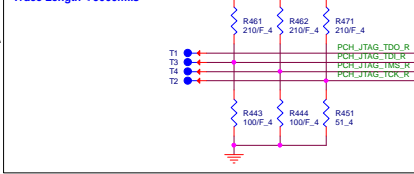


HDA

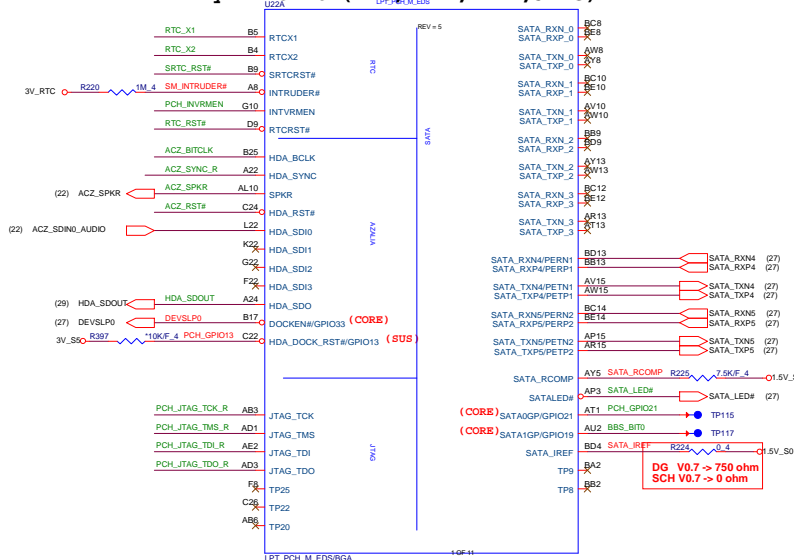


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



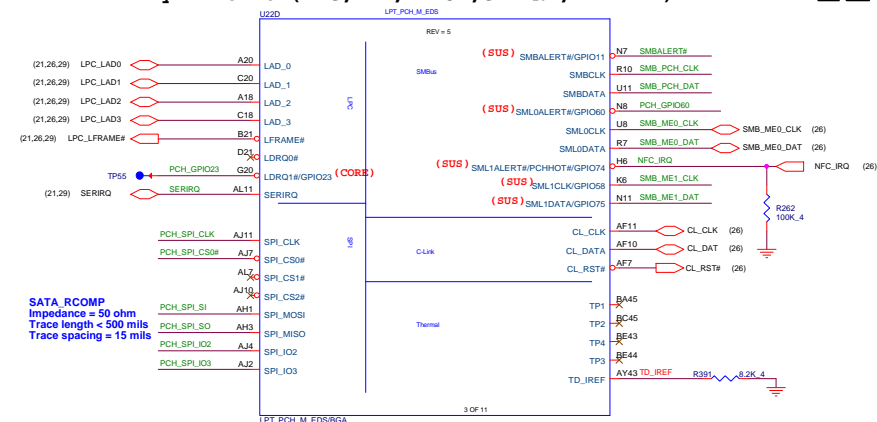
Lynx Point (RTC, IHDA, SATA, JTAG)



PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	(11) ACZ_SPKR R260 *10K_4 Q3V_S0
GPIOE2 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(11,26) SUSCLK R254 *1K_4
GPIOS5	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(11) STP_A16QVR R259 *37K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	(11) PCH_INVNRM R214 330K_4 Q3V_RTC
GPIOS1	Boot BIOS Strap bit 1	PWROK	Bit1 B10 0 = Reserved 1 = Reserved	(11) BBS_B11 R415 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK	0 = BBS_57D 1 = BBS_57D	(11) BBS_57D R464 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	HDA_SDOOUT R215 *1K_4 Q3V_S5 R216 *20K_4
SATA2GP/GPIO36	RSVD	PWROK	Internal PD	(14) PCH_GPI36 R430 *200K_4 Q3V_S0
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(14) PCH_GPI37 R472 *1K_4 Q3V_S5
GPIO8	RSVD	RSMRST#	Internal PU	(14) PCH_GPI08 R438 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(11) DSWVREN R224 330K_4 Q3V_RTC

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)



HDD

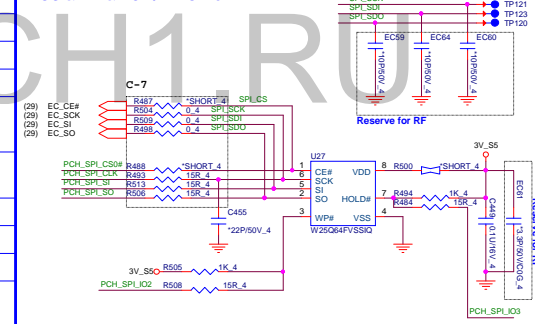
ODE

SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

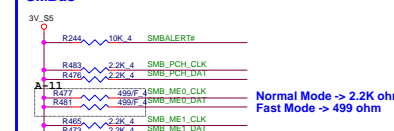
Pull High



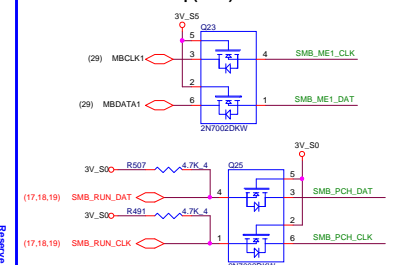
PCH Dual SPI
BIOS & ME & EC F/W ROM 8MB



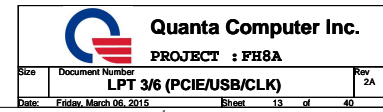
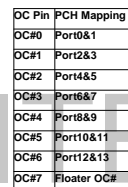
SMBus

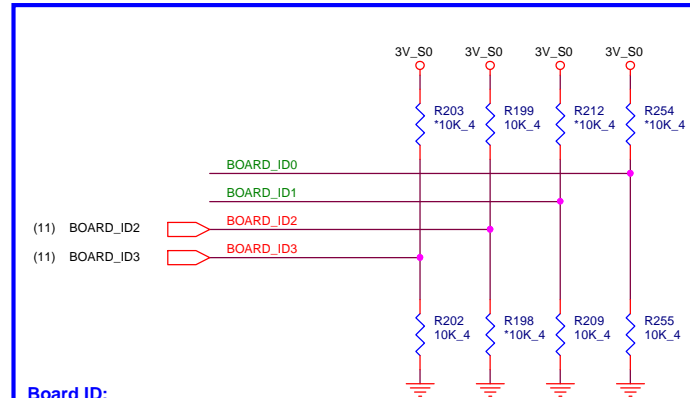
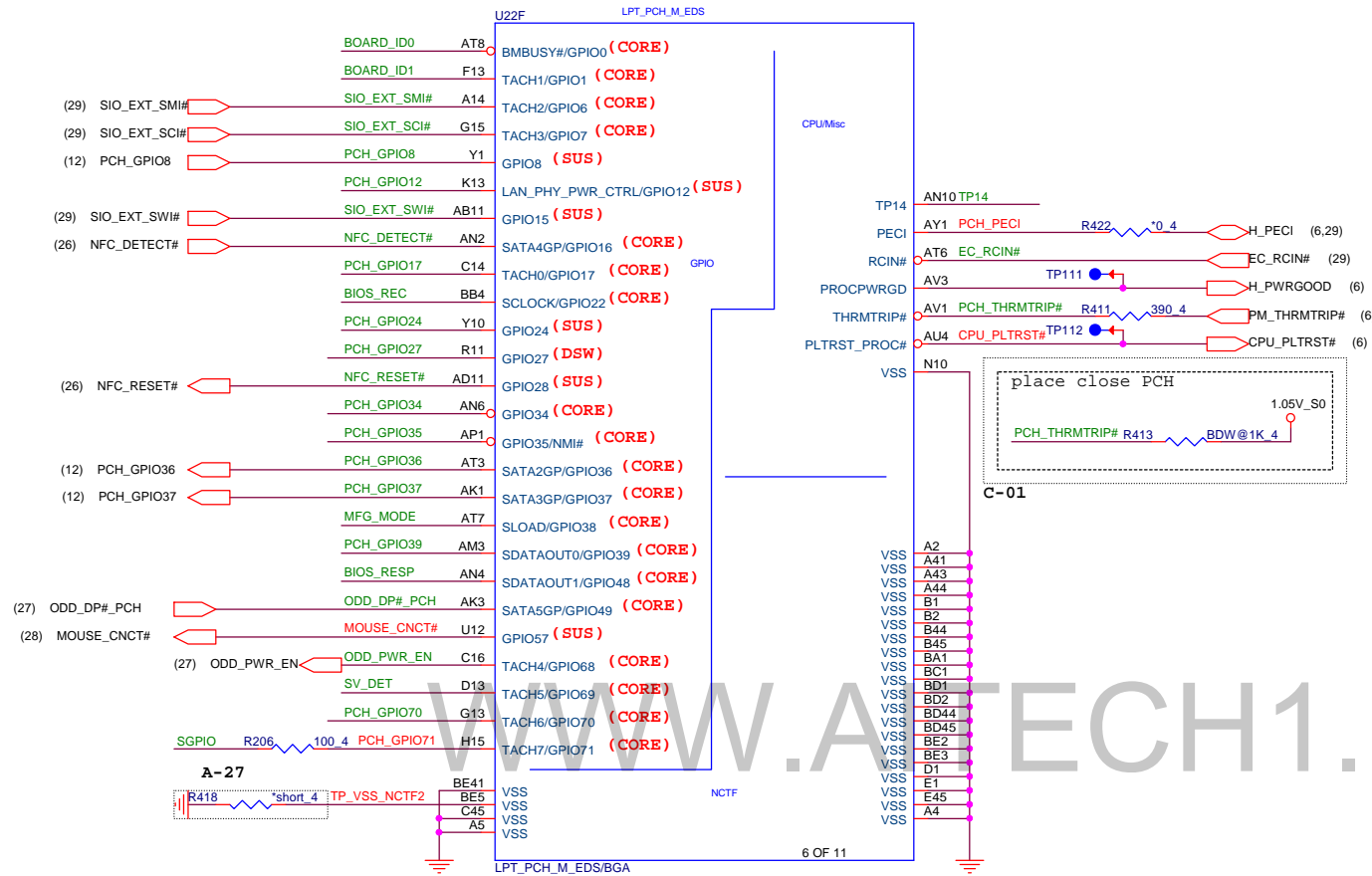


SMBus/Pull-up(CLG



Lynx Point (CLOCK)





Board ID:

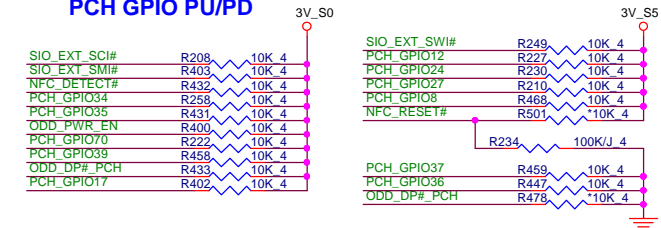
BOARD_ID0	PCH_CPIO0
UMA	0
DIS	1

BOARD_ID3	PCH_CPIO4
Touch	0
Non-touch	1

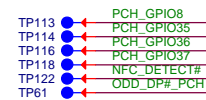
BOARD_ID1	PCH_CPIO1
LVDS	0
eDP	1

BOARD_ID2	PCH_CPIO3
VGA	0
non-VGA	1

PCH GPIO PU/PD



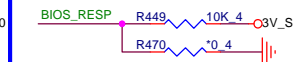
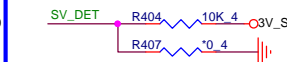
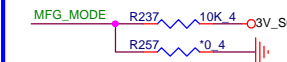
XDP Signal



PCH MISC PU/PD

BIOS RECOVERY 0 = Enable
1 = DisableSwap GPIO 0 = SGPIO
1 = Default

MFG TEST

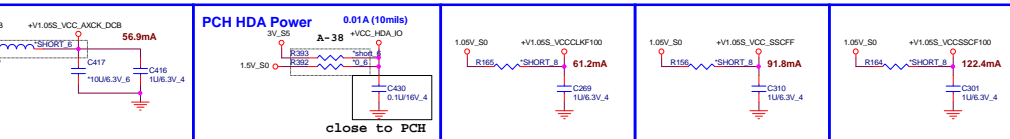
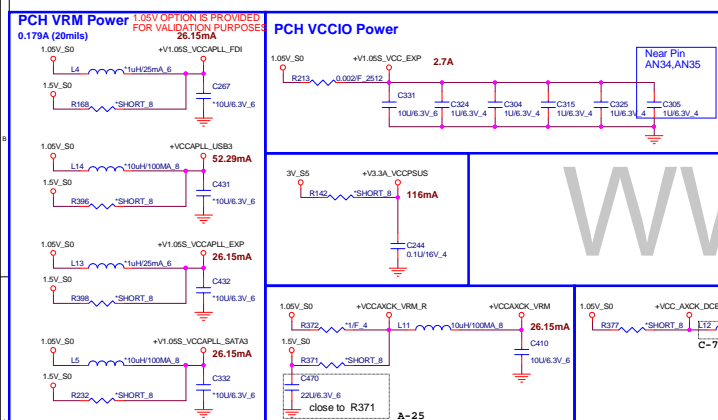
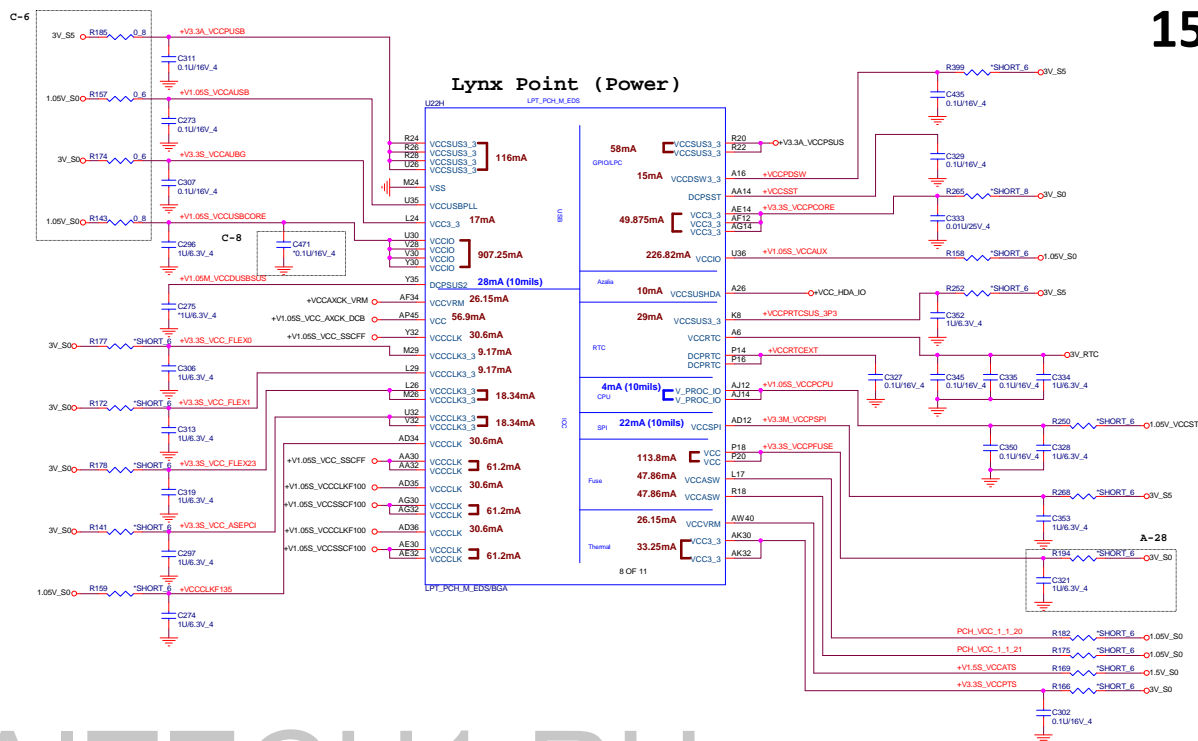
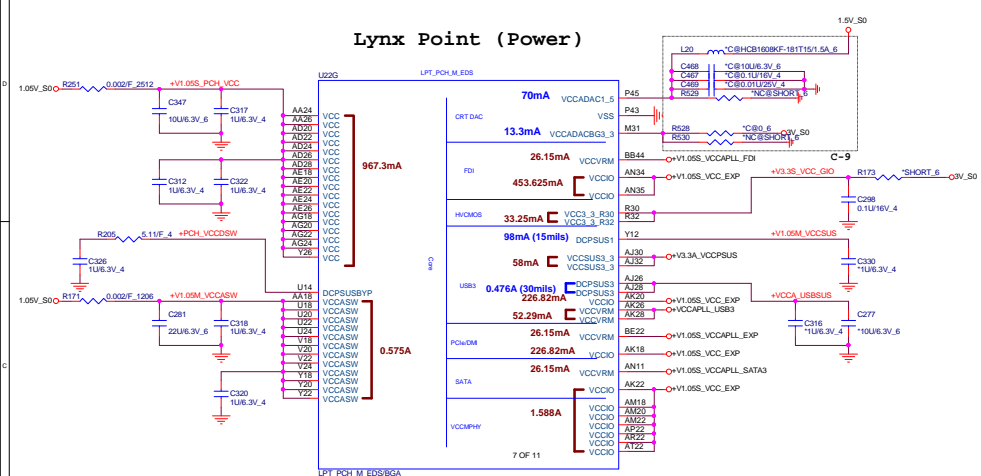
SV Detect 0 = SV Detect
1 = DefaultBIOS_RESP 0 = BIOS RESP
1 = Default

Quanta Computer Inc.

PROJECT : FH8A

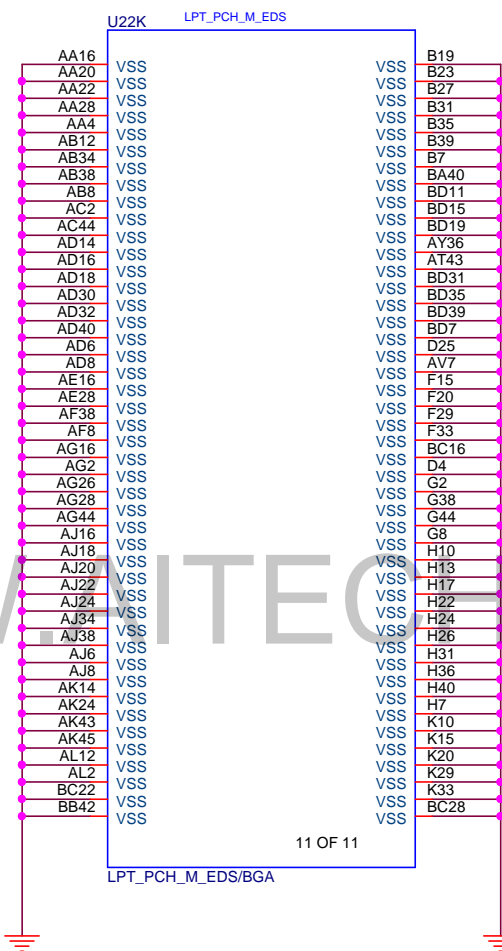
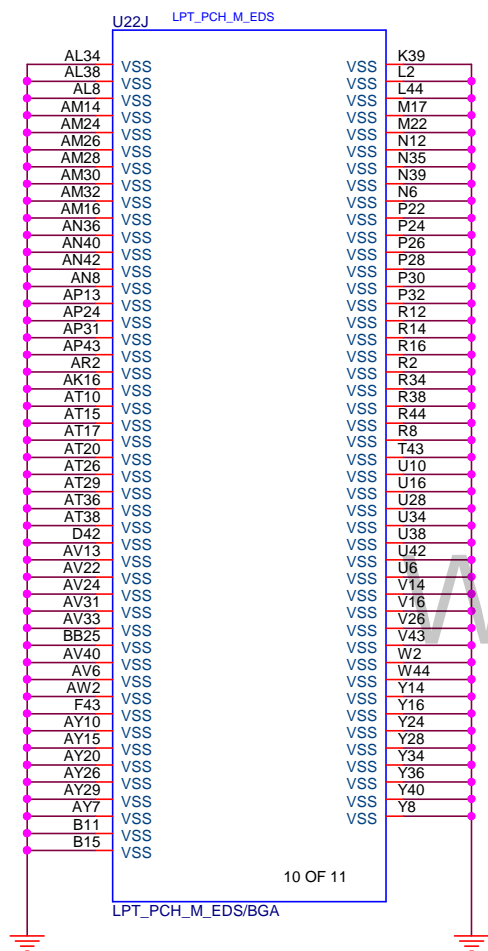
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Date: Friday, March 06, 2015 Sheet 14 of 40



Lynx Point (GND)

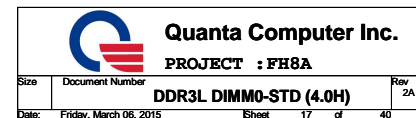
Lynx Point (GND)

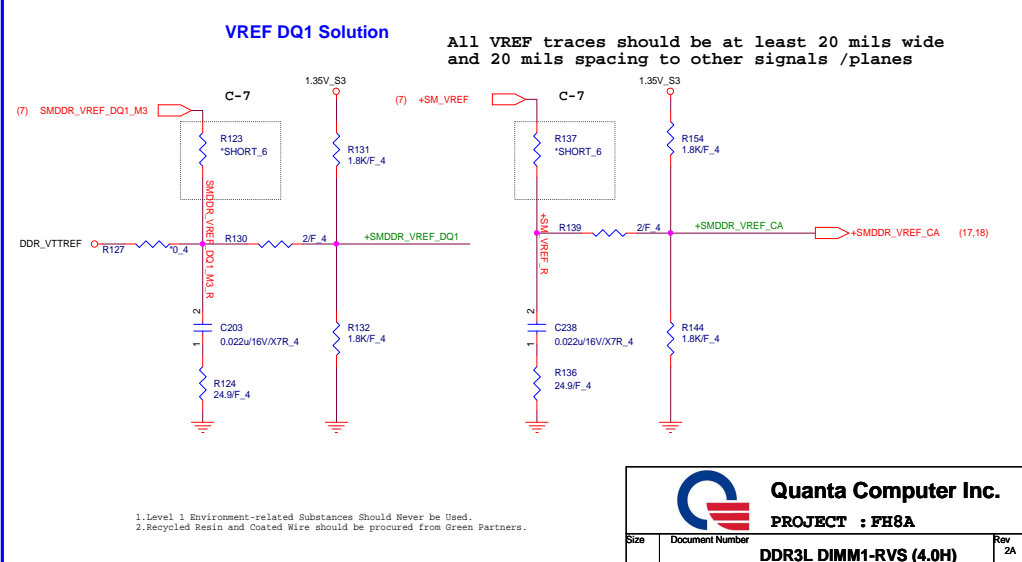


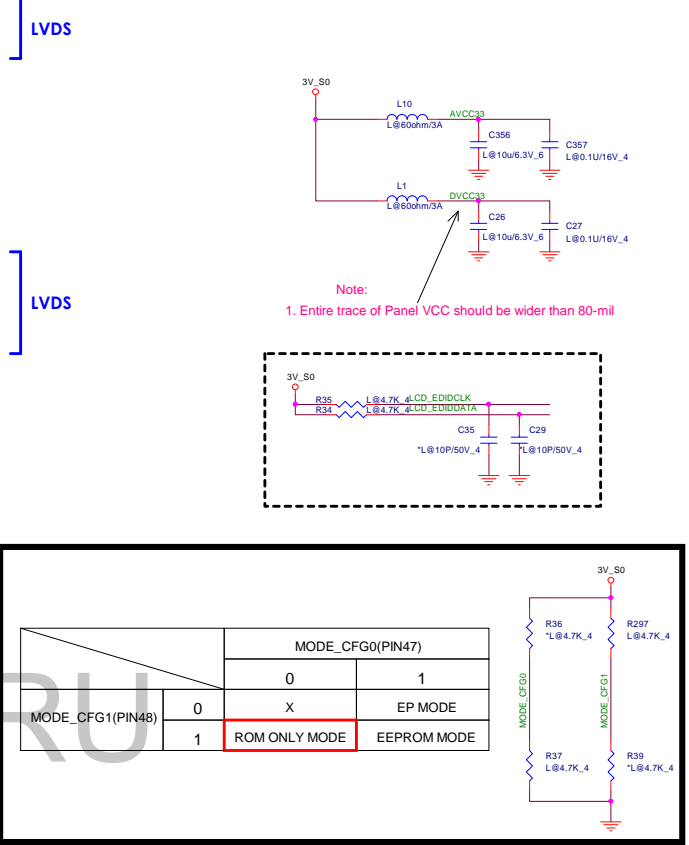
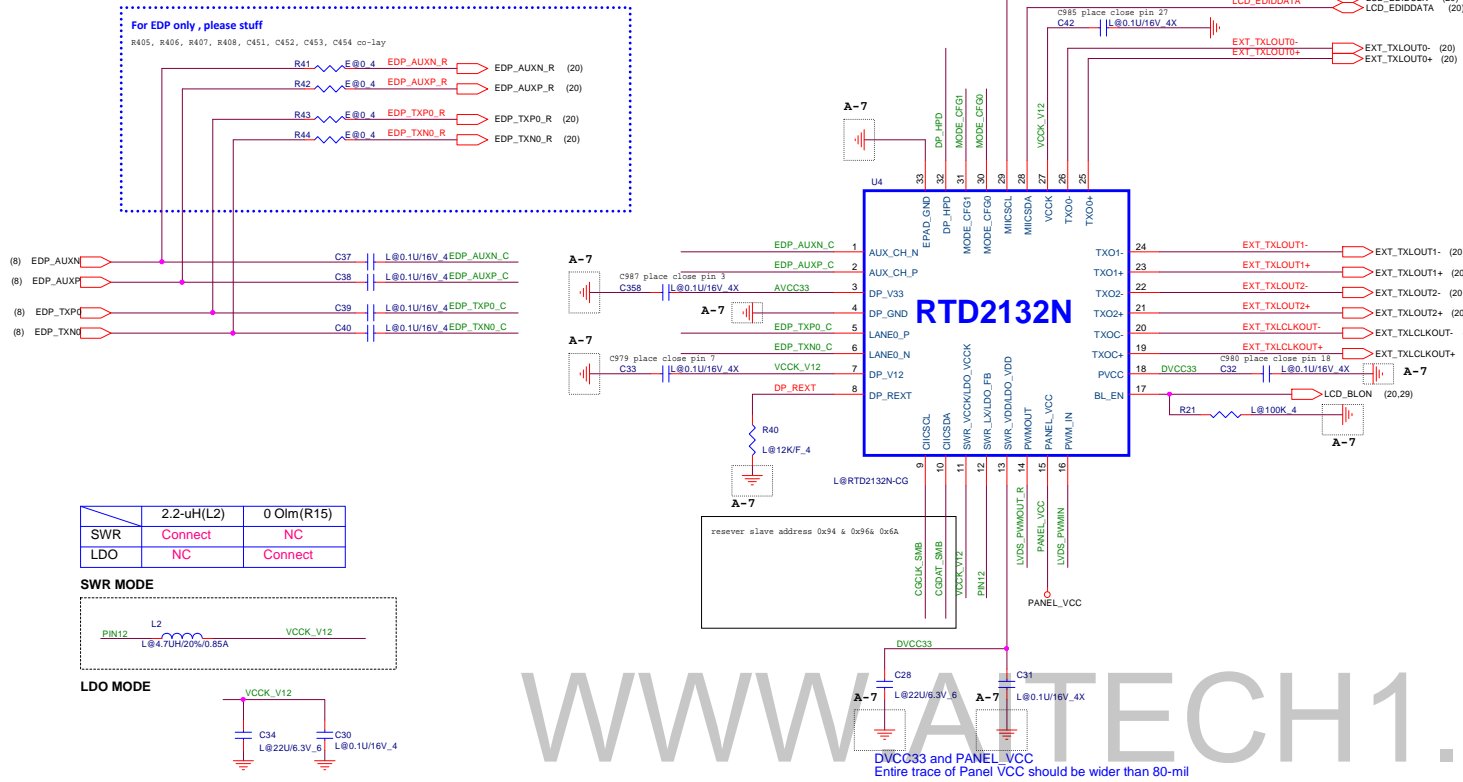
Quanta Computer Inc.

PROJECT : FH8A

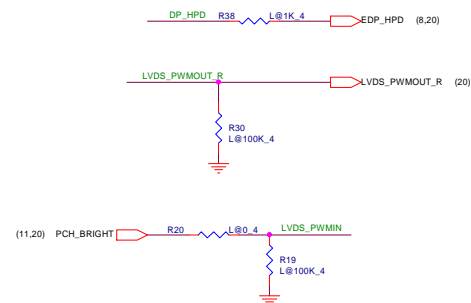
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Date:	Friday, March 06, 2015	Sheet 16 of 40



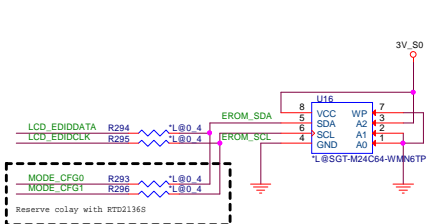




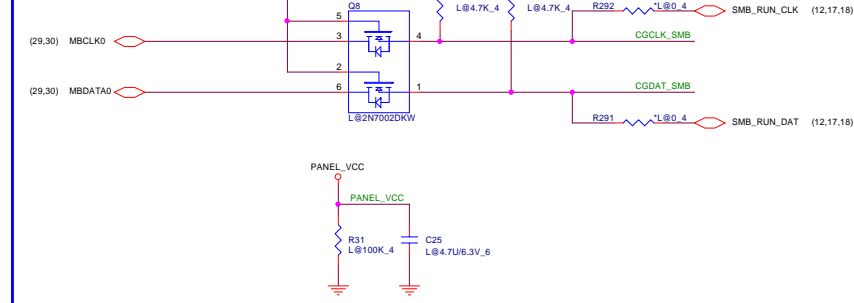
HPD/ Back Light/ BL PWM

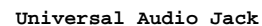
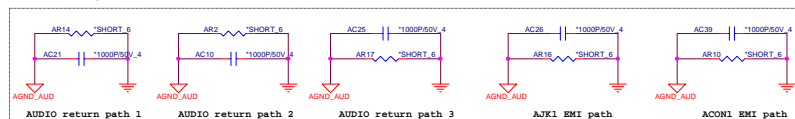
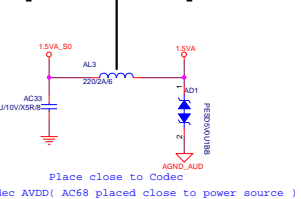
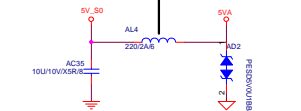


Reserve EEPROM Address=0xA8

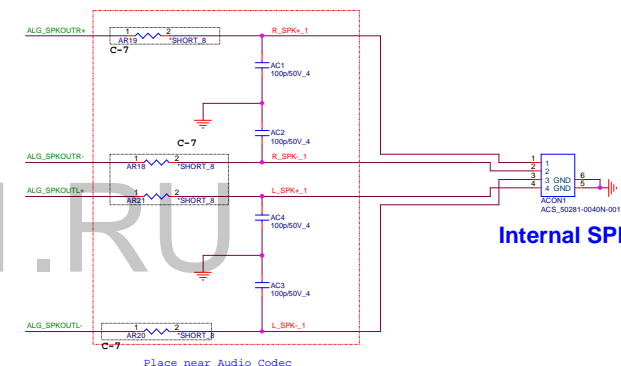
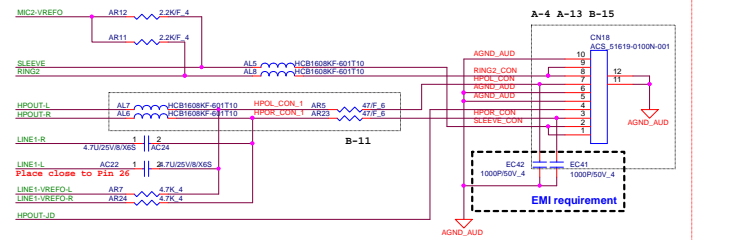


SMBUS & Panel VCC

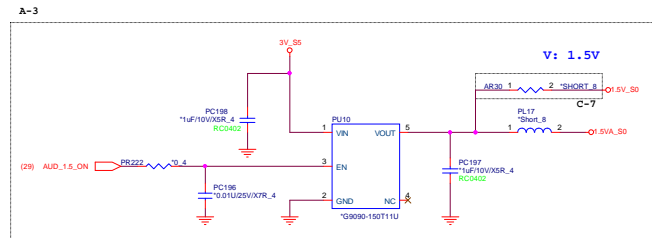




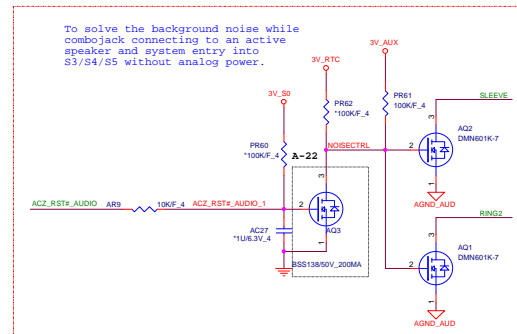
(ALC283 supported iPhone/Nokia headset, Headphone, Line-In and Microphone)

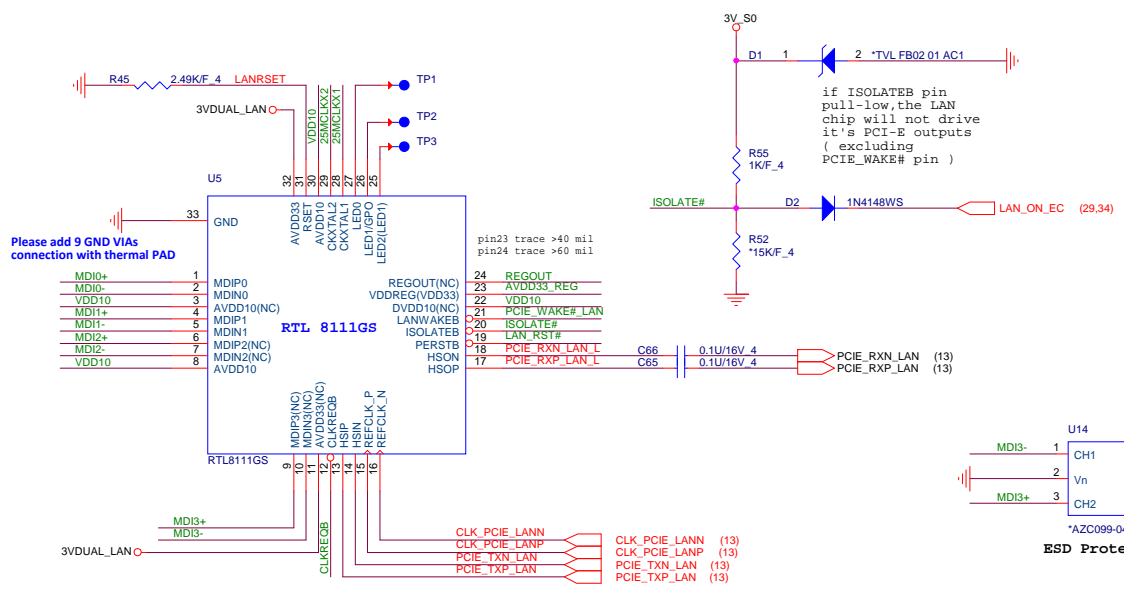


Internal SPK



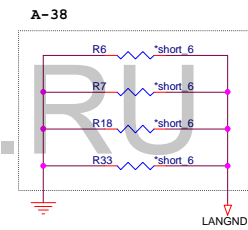
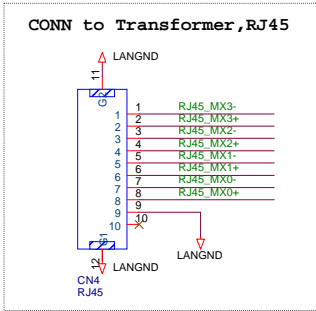
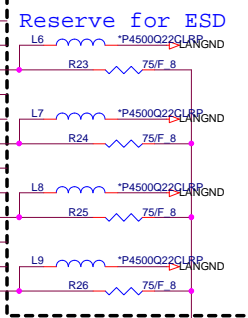
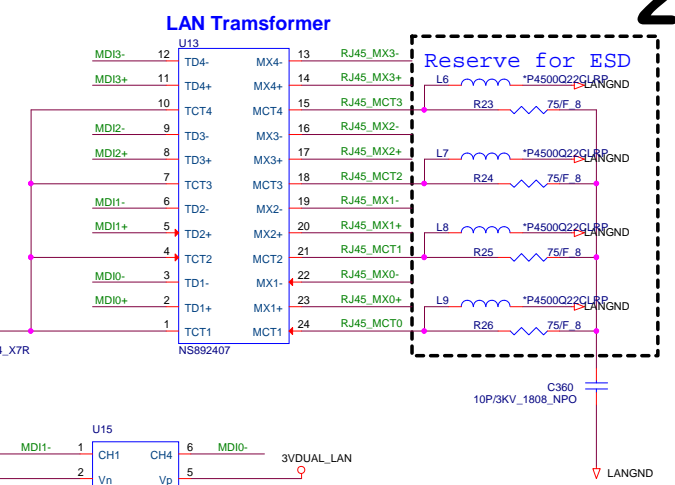
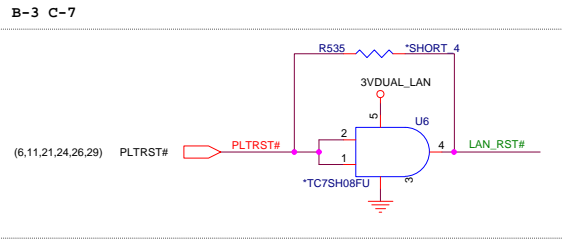
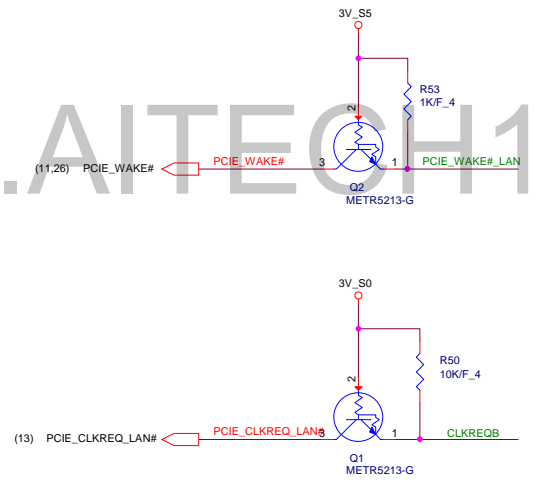
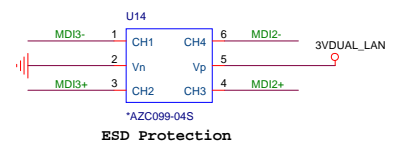
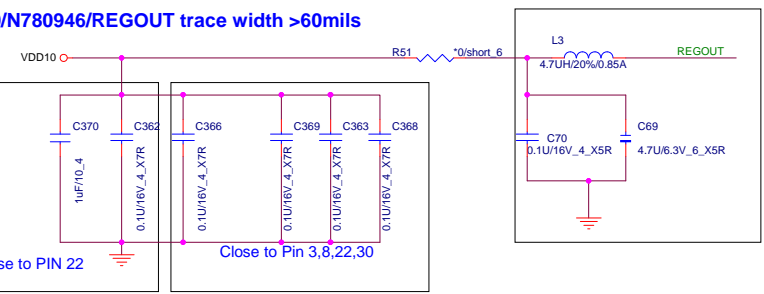
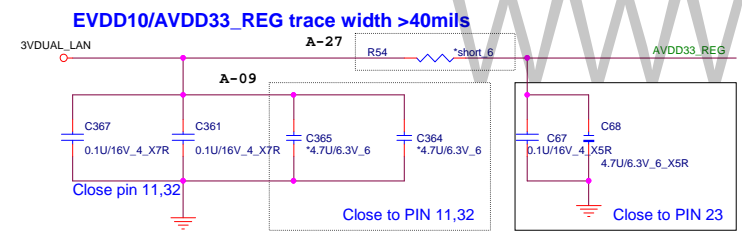
5/28 upadted





Please add 9 GND VIAs connection with thermal PAD

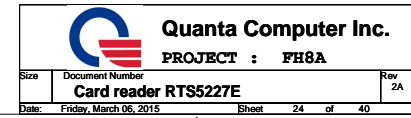
LAN POWER



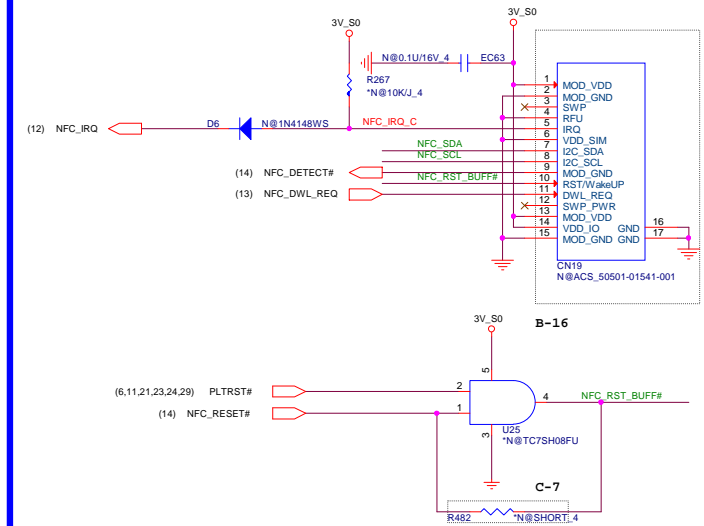
X'tal 25MHz

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PROJECT : FH8A
LAN RTL8111GS/RJ45 conn

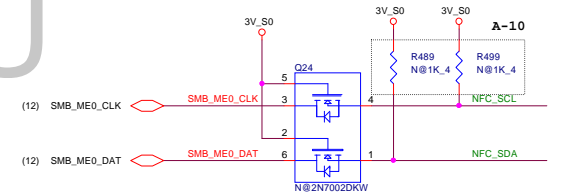
Size Document Number
Date: Friday, March 06, 2015 Sheet 23 of 40



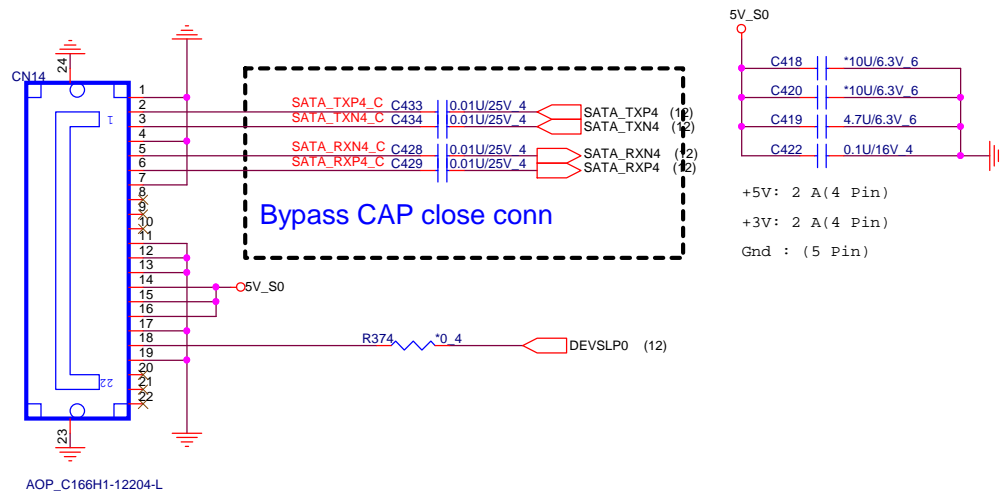
26



TO PWR/B

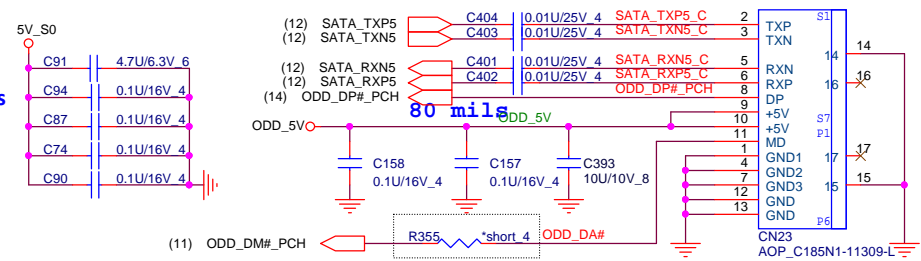


SATA HDD Connector



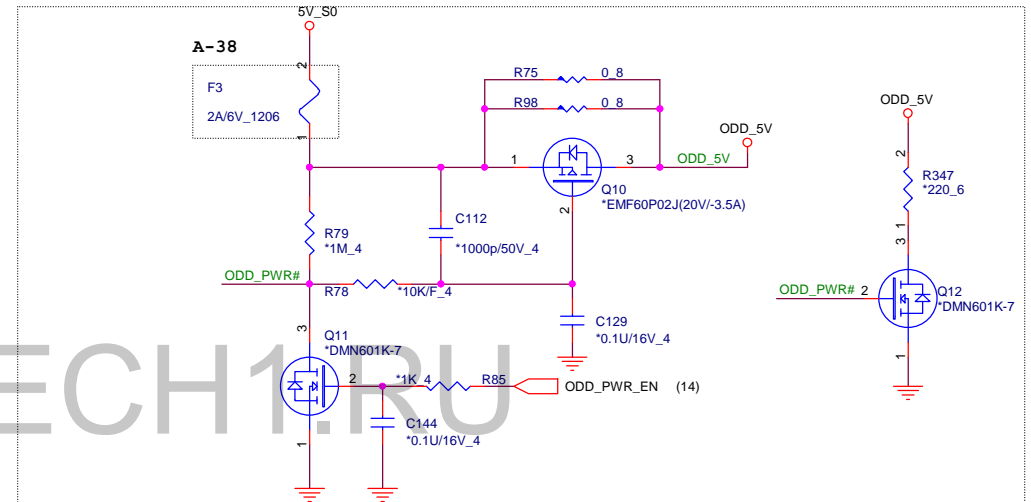
SATA ODD Connector

120 mils



MP1-01

A-27



LED

B-2

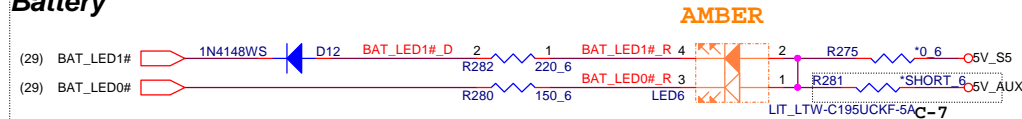
CAPS LED



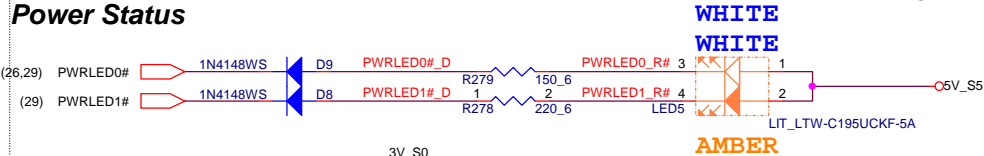
WLAN



Battery



Power Status



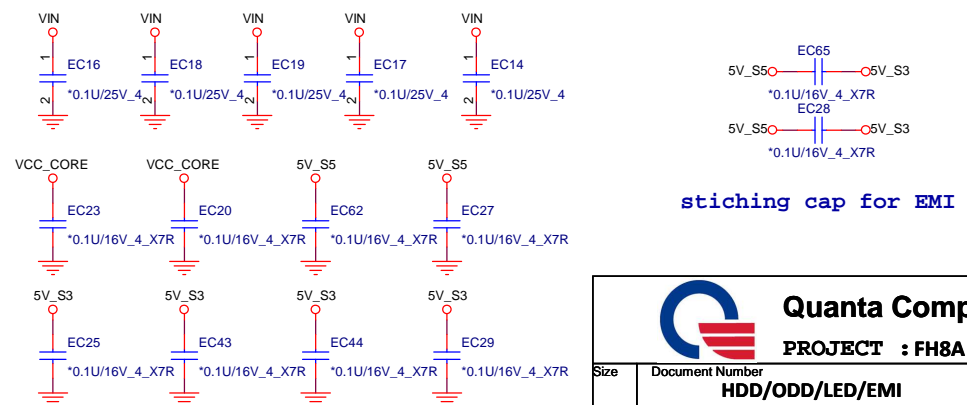
HDD/ODD



NUM LED



EMI

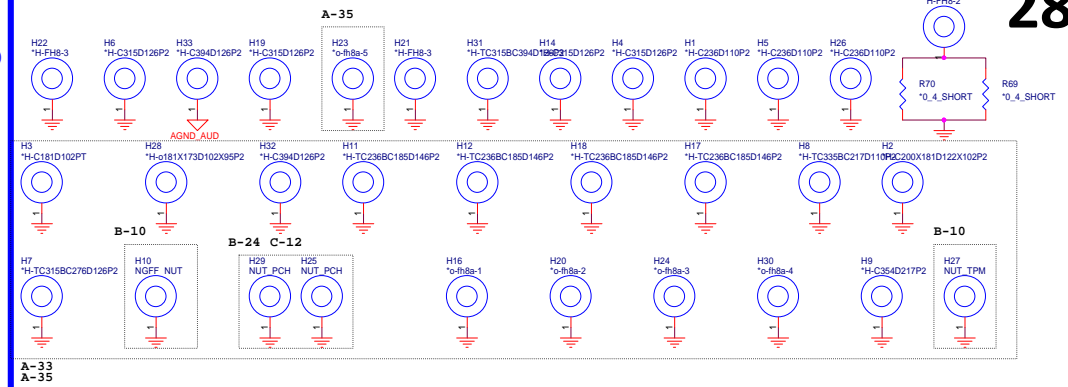


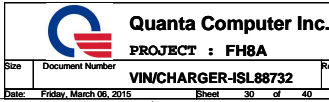
Quanta Computer Inc.

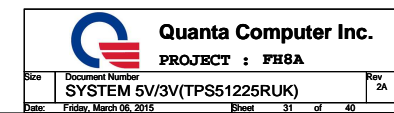
PROJECT : FH8A

Size	Document Number	Rev
	HDD/ODD/LED/EMI	2A
Date:	Friday, March 06, 2015	Sheet 27 of 40

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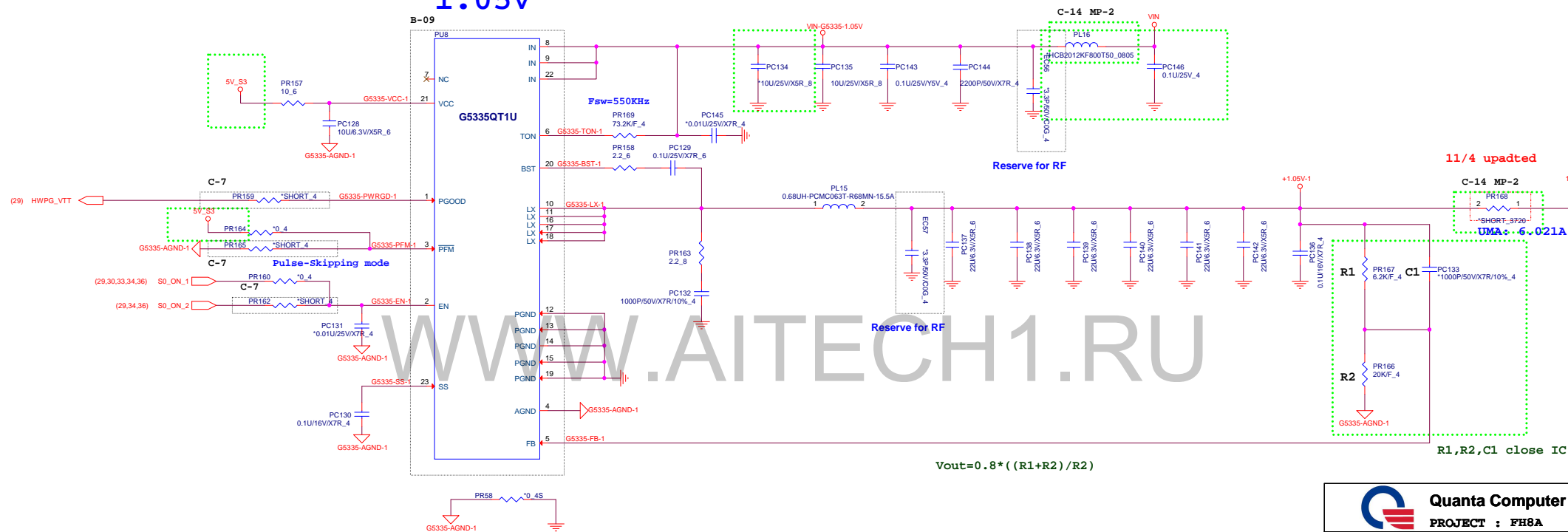
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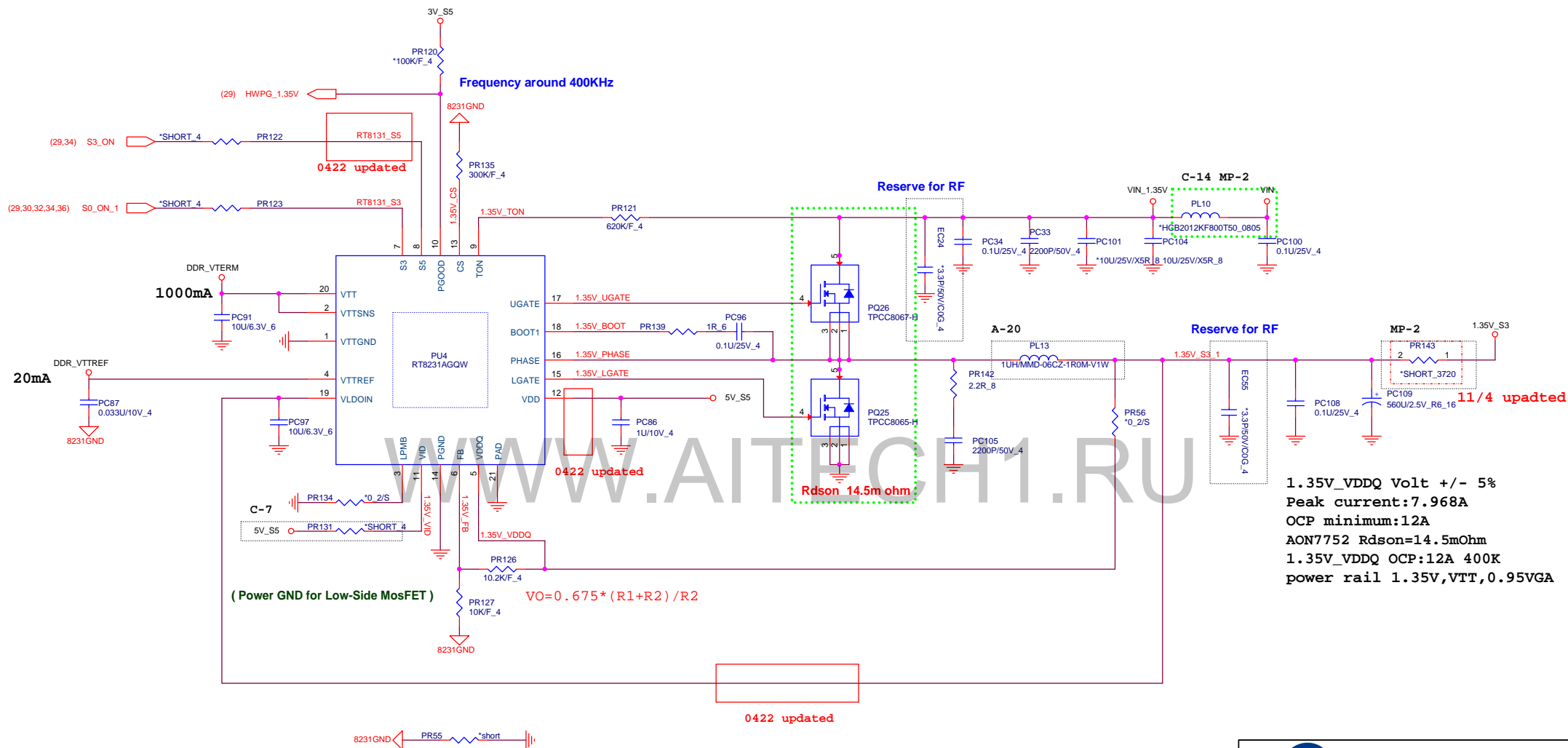


+1.05V

1.05V

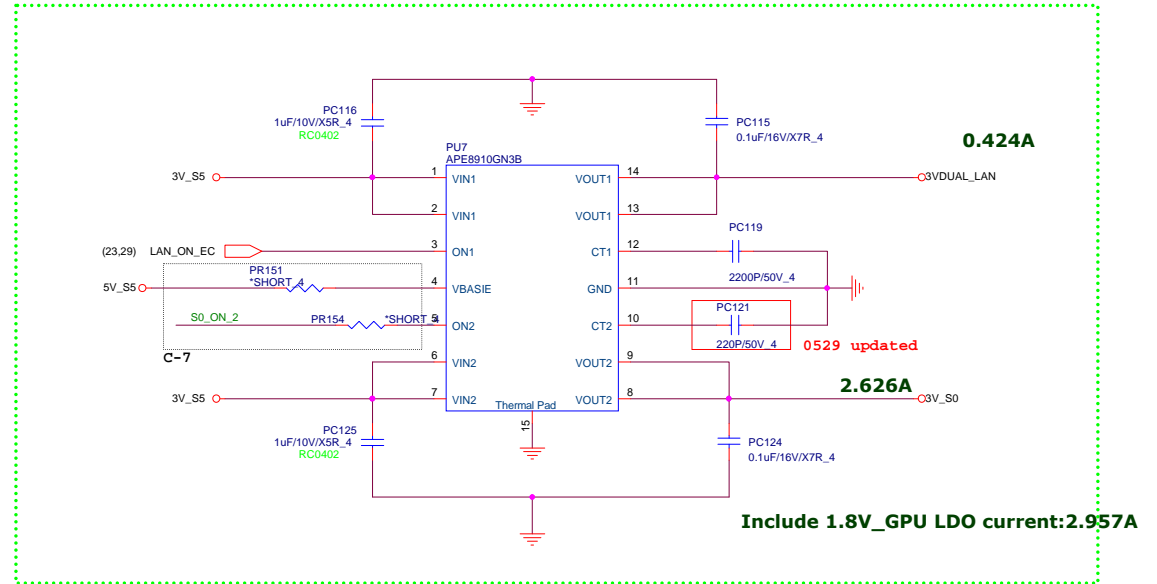
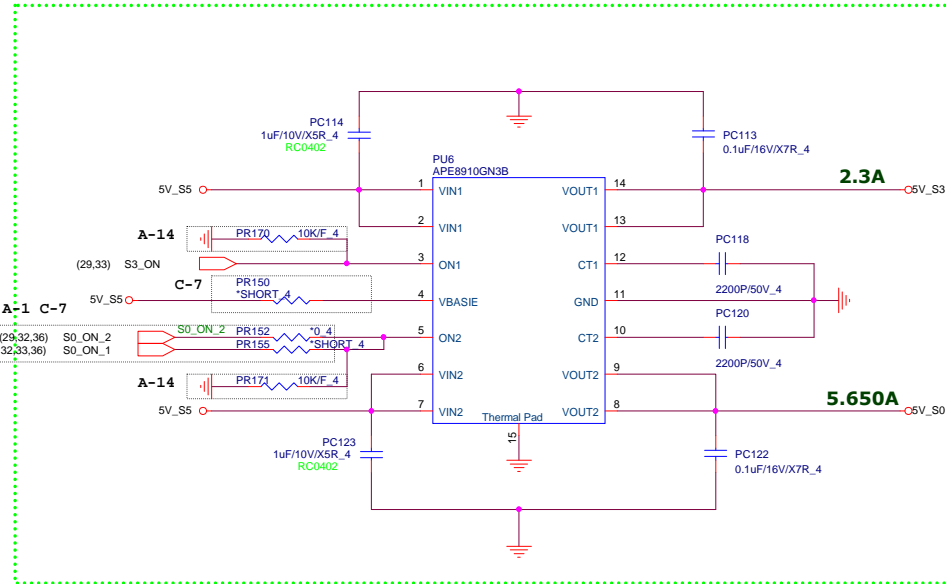


1.35V_VDDQ (RT8231AGQW)

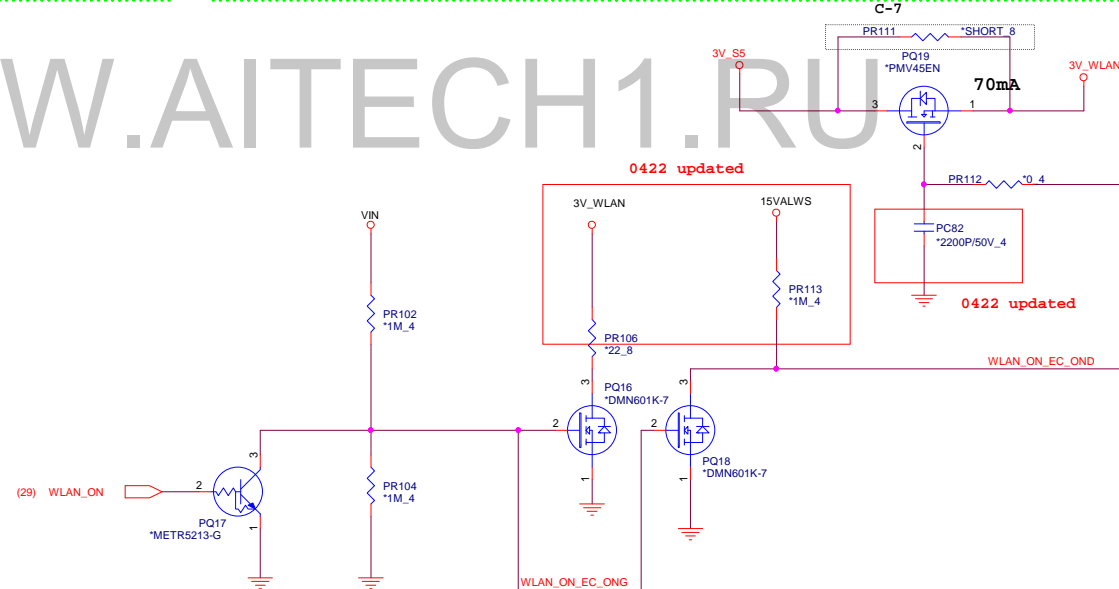
**Quanta Computer Inc.**

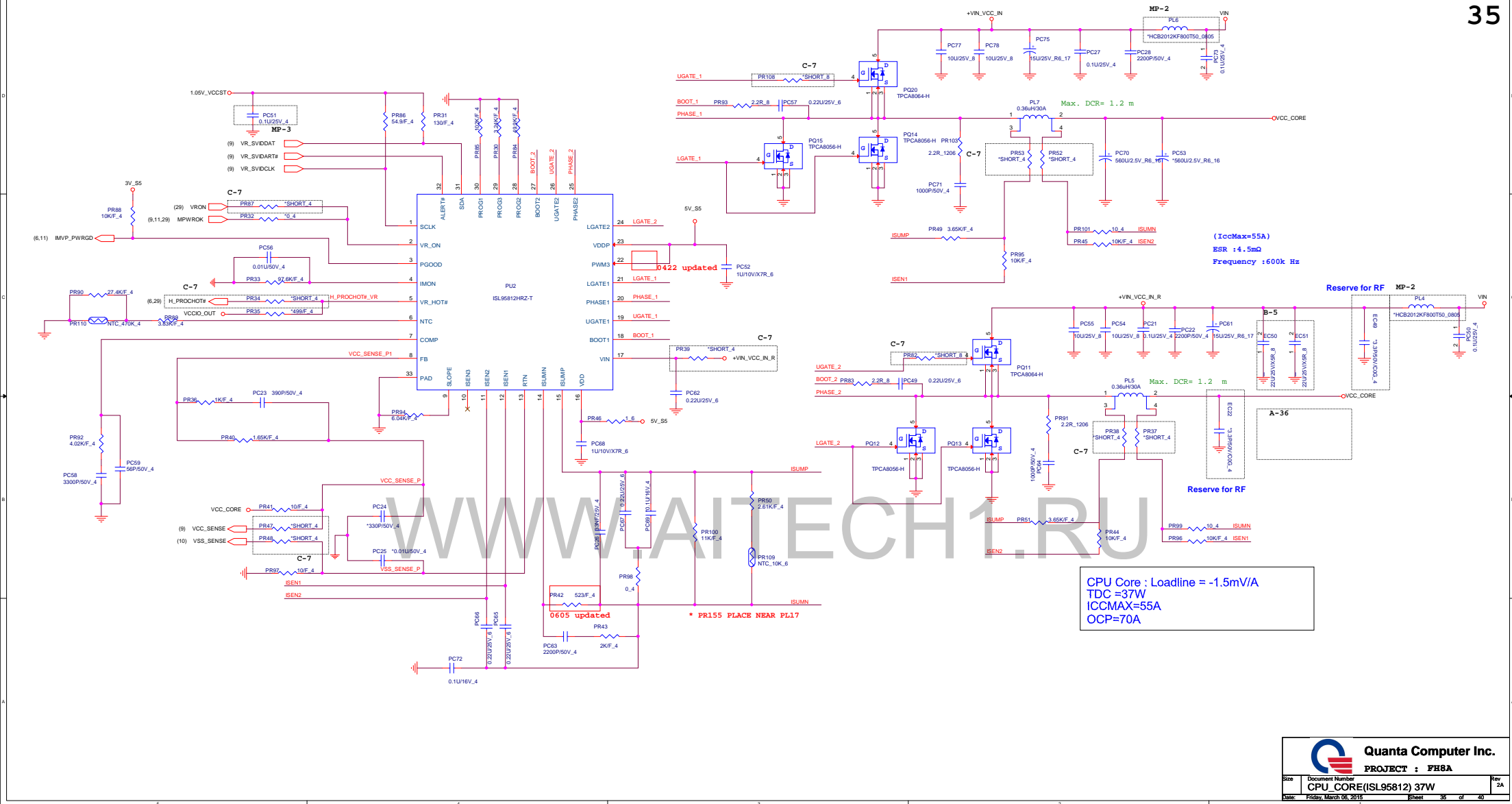
PROJECT : FH8A

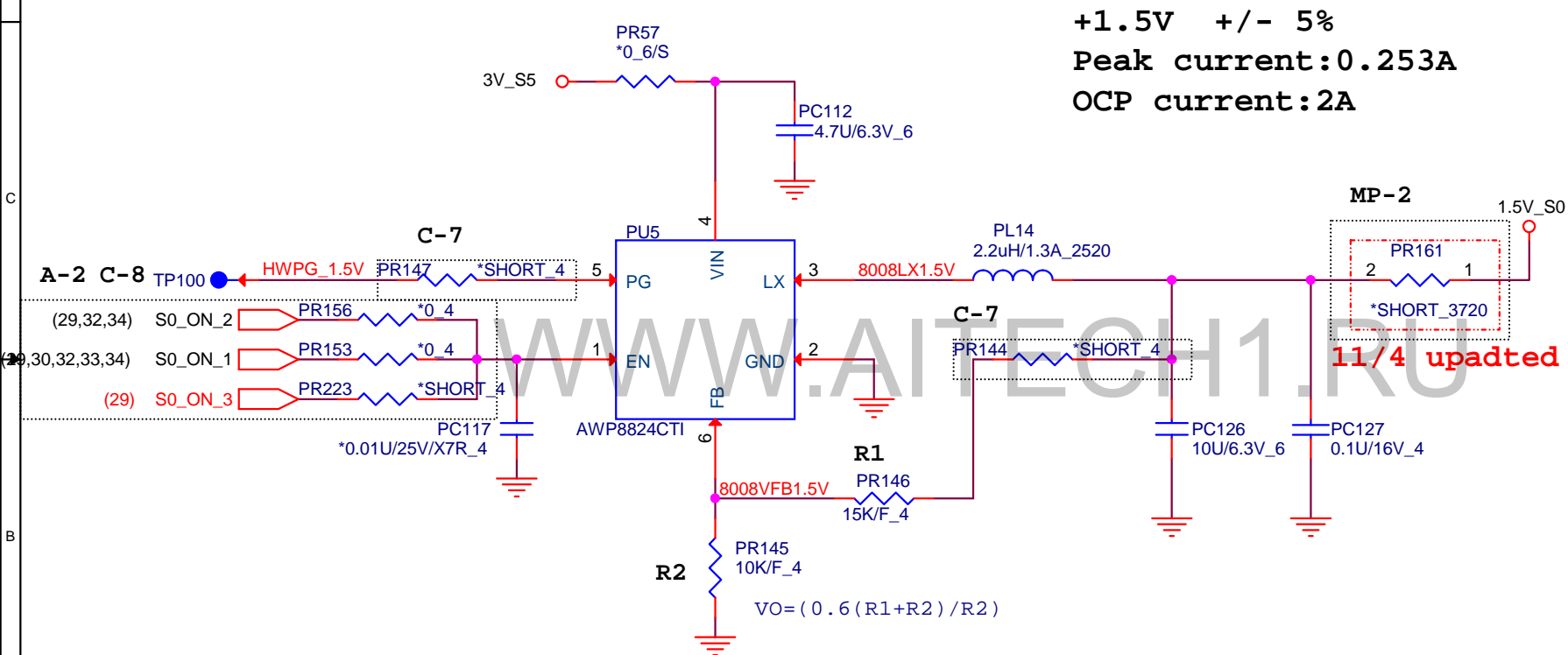
Size	Document Number	Rev
	DDR3L 1.35V(RT8231AGQW)	2
Date:	Friday, March 06, 2015	Sheet 33 of 40



WWW.AITECH1.RU







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PROJECT : FH8A

Size

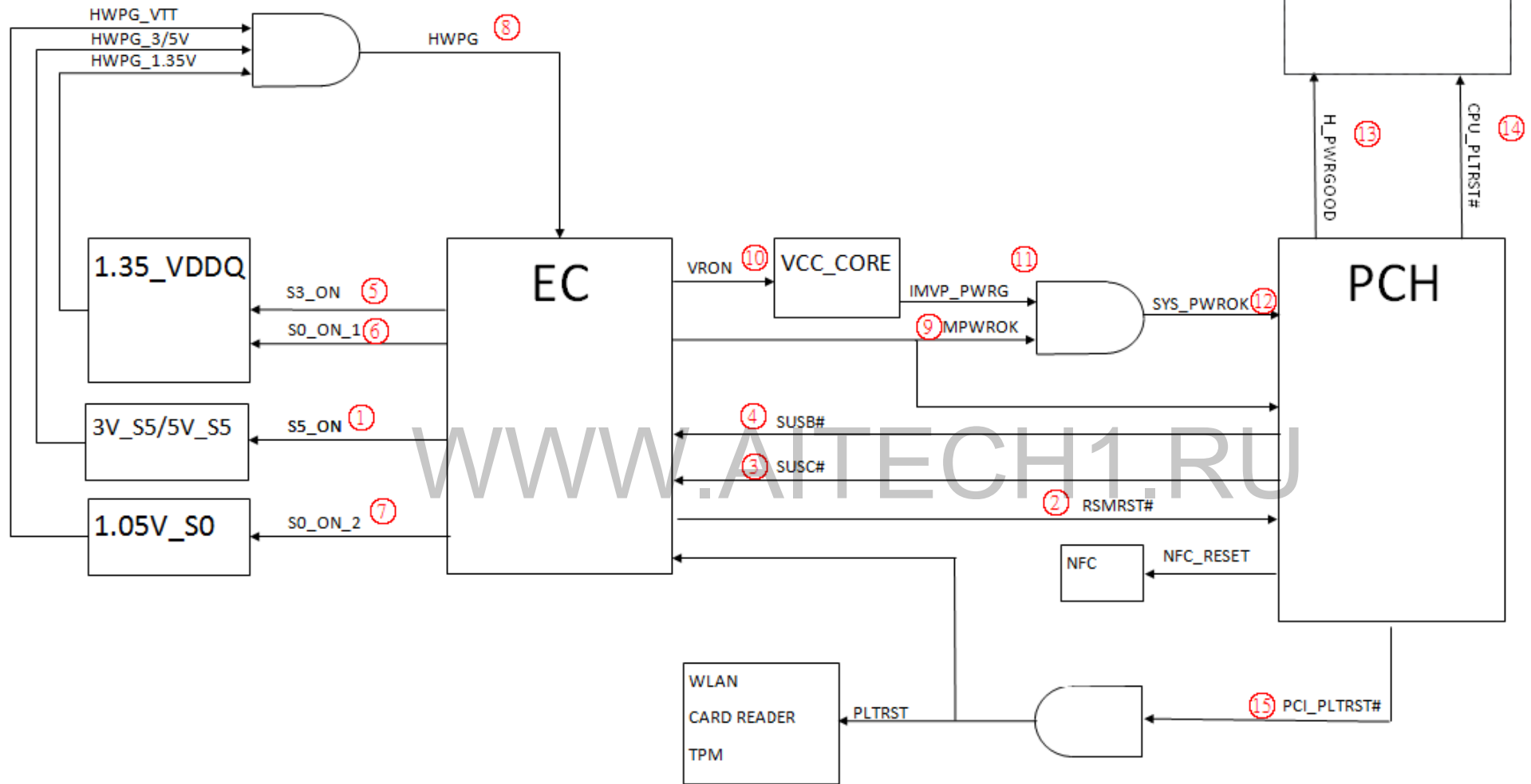
Document Number

Rev
2A

1.5V_S0

Date: Friday, March 06, 2015

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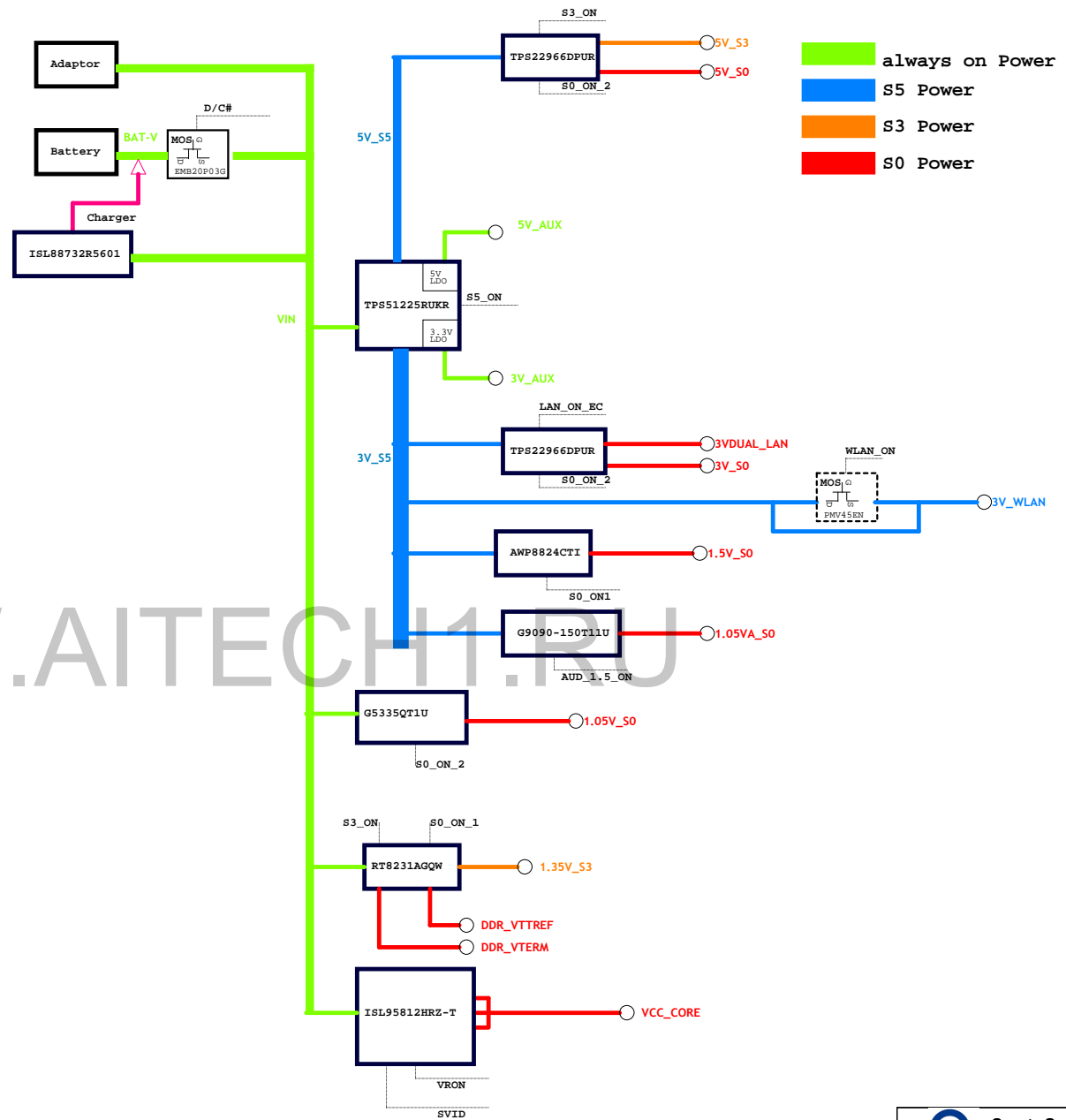


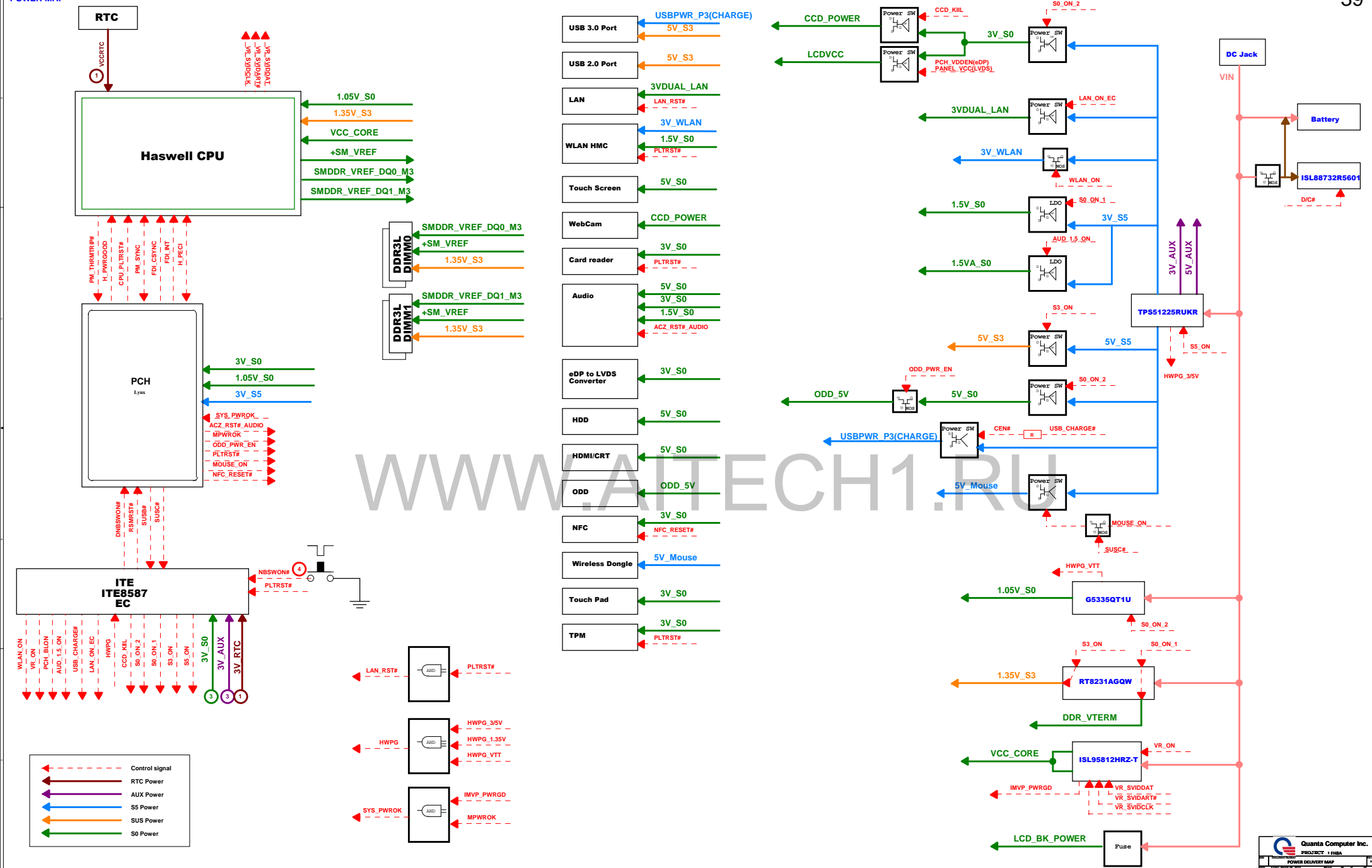
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Size	Document Number	Rev
	RESET/PWROKMAP	2A
Date:	Friday, March 06, 2015	Sheet 37 of 40

Power Rail	Destination	Voltage
VCC_CORE	CPU VCC ---- Processor core power rail.	
1.5V_S0	PCH: VCCPLL ---- for VCCPLL provides isolated power for internal PCH PLLs PCH : +VCCAXCK_VRM for 1.5V power supply for VCC_VRM HDMI LEVEL SHIFTER : VDDTX/RX for level shifter TX/RX power Mini PCIE : +1.5V(WLAN) AUDIO : +1.5VA --- for Codec AVDD2 AUDIO : +AZA_VDD --- for Codec DVDDIO	
1.35V_S3	CPU: I/O supply voltage for DDR3L. DIMM : DDR3L power	
DDR_VTERM	DDRIII Terminator:	
1.05V_S0	PCH : PCH VccCore PCH : VccASW --- +V1.05M_VCCASW for the Active Sleep Well PCH : +V1.05S_VCCUSB CORE ---USB core PCH : +V1.05S_VCCCAUX: VCCIO for GPIO/LPC IO PCH : VCCIO ---+V1.05S_VCC_EXP for FDI voltage PCH : VCCIO ---+V1.05S_VCC_EXP for USB3 voltage PCH : VCCVRM ---+V1.05S_VCCAPLL_EXP for SATA PCH : VCCIO --- +V1.05S_VCCAPLL_EXP for SATA PCH : VCCIO --- +V1.05S_VCCAPLL_EXP for VCCMPHY PCH : VCCVRM ---+VCCAXCK_VRM for ICC PCH : VCC ---+V1.05S_VCC_AXCK_DCB for ICC PCH : VCCCLK --- +VCCCLKF135 for ICC PCH : VCCCLK --- +V1.05S_VCC_SSCFF for ICC PCH : VCCCLK --- +V1.05S_VCCSSCF100F for ICC PCH : VCCST POWER GREEN CLOCK : VIOE_25MB: for PCH 25 CLOCK VDD	PCH :VCCIO: +V1.05S_VCCCAUX for GPIO/LPC PCH :VCCASW: PCH_VCC_1_1_20/21 for FUSE CPU : VCCIO_OUT --- +VCCIO_OUT_R CPU : VCCST: 1.05V_VCCST
3V_AUX	PCH: RTC EC: VSTBY KB : KB ID KB : KB ID MMB : MMB VDD HALL SENSOR : SENSOR VDD	
3V_S5	PCH: VccSus3_3 -- +VCCPRTCSUS_3P3forRTC. PCH:VCCDSW3_3 -- +VCCPDSW supply for Deep S4/S5 wells. PCH:VCCSPI -- +V3.3M_VCCPSPI for SPI PCH:VCC -- +V3.3S_VCCPFUSE for PCH fuse SPI ROM : VCC for SPI ROM WLAN: 3V_WLAN for WLAN VCC	PCH : VCCSUSHDA ---- +VCC_HDA_IO for Azalia Power. PCH :VCCSUS3_3 ---- USB3/USB2 SUS power,
3V_S0	PCH: Vcc3_3 --- for core well I/O buffers. PCH: Vcc3_3_R30/R32 --- for HVC MOS PCH: VCCCLK3_3 --- for ICC. PCH: VCC --- for FUSE. PCH: Vcc3_3 --- for THERMAL. DDR3: SPDVDD VGA Port Companion Circuit HDMI LEVEL SHIFTER POWER LVDS power CCD power	TOUCH PAD POWER TPM power Card reader(RTS5227E)power NFC POWER EC: VCC
3V_WLAN	Mini PCIE : 3V power	
3VDUAL_LAN	LAN Power	
5V_AUX		
5V_S5	USB CHARGER : USB CHARGER POWER WL DONGLE: WL DONGLE POWER	
5V_S3	USB2.0 power TTOUCH SCREEN POWER	
5V_S0	FAN power HDMI power pin HDD power ODD power Audio codec IC power VGA power pin	
VIN	CONVERTER power	
BAT-V		





Item	Stage	Page	Owner	Change explanation
				B Stage
01	A -> B	01	RM	Current block diagram description from Boardwalk to Hawaii-1
02	A -> B	27	RM	Change R27J224, R27J7, R27J, R27J, R27J to 15 Ohm for the AWB chipwires.
03	A -> B	27	RM	Change C63 to DFCPCAP63 for ASLT. Use the same AWB connector types.
04	A -> B	30,35	RM	Change the R570 and R531 and de-pop R530 for SM Lense.
05	A -> B	20,21,25,26	RM	Delete R248,R249,R246,R287,R373,R375,R316,R421,R430,R490,R369,R323,L24 for SMT support. Support Q32 and add R370 for CDR CMOS Tuning
06	A -> B	14	RM	
07	A -> B	22	RM	Change R2F033, R2E, C45F, R2B1 to shorted CDR C70
08	A -> B	22	RM	
09	A -> B	27	RM	Delete R274 and R235 for battery Load power
10	A -> B	22	RM	Delete R26, R41, R42 for V2 C/D
11	A -> B	28	RM	Change R26, R41, R42 to R-V2C17C81814492, R27 to R-V2C17C817915092
12	A -> B	22	RM	ASLT / R232 swap with ASLT / ASLT for audio pop noise.
13	A -> B	22	RM	Change R242, R245, R244, R216, R217 to audio pop debug.
14	A -> B	28	RM	CM8 change PM to DFCPC1P2212 & DFCPC1P2050 , and P/F to 50501-01201-001-12p-1 for MM request.
15	A -> B	28	RM	CM8,CM10 change PM to DFCPC0P2053 & DFCPC0P2055,P/F to 50501-0080n-001-1p-1 for MM request.
16	A -> B	22	RM	CM8 change PM to DFCPC10P213,P/F to 51616-0100n-001-10p-1 for MM request.
17	A -> B	26	RM	CM10 change PM to DFCPC1P2010 & DFCPC1P2011 , P/F to 50501-01541-001-15p-1 for MM request.
18	A -> B	26	RM	CM10 change PM to DFCPC0P212,P/F to 50504-0560n-001-6p-1 for MM request
19	A -> B	21	RM	CM8 add 2nd pin group ZN DFCPC94P219 for MM request
20	A -> B	21	RM	CM8 change to DFCPC0P216 & DFCPC0P217 for MM request
21	A -> B	23	RM	CM4 change to DFCPC0P217 & DFCPC0P218 , P/F to 50573-01001-001-10p-1 for MM request
22	A -> B	24	RM	CM1 DFCPC110P208 R26, P/F to 50501-0241-001-12p-16p for SMT add Mylar
23	A -> B	20	RM	Change P1 to DFC0P0P004 & DFC0P0P004 for STD part.
24	A -> B	11	RM	Change N55,N52 to N52R002010 for MC change.
25	A -> B	12	RM	Use -stuff R2426,C442,C442 for cancel reserve X'al Function.
26	A -> B	12	RM	
27	A -> B	12	RM	
28	A -> B	12	RM	
29	A -> B	12	RM	
30	A -> B	12	RM	
31	A -> B	12	RM	
32	A -> B	12	RM	
33	A -> B	12	RM	
34	A -> B	12	RM	
35	A -> B	12	RM	
36	A -> B	12	RM	
37	A -> B	12	RM	
38	A -> B	12	RM	
39	A -> B	12	RM	
40	A -> B	12	RM	
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43	A -> B	12	RM	
44	A -> B	12	RM	
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74	A -> B	12	RM	
75	A -> B	12	RM	
76	A -> B	12	RM	
77	A -> B	12	RM	
78	A -> B	12	RM	
79	A -> B	12	RM	
80	A			

Item	Stage	Page	Owner	Change explanation
				C stage
16	B -> C	25	EN	change U23 to B082047PQ3-GK2 for DCP to 2.5A.
17	B -> C	20	EN	change U29 to 02R8407 for HMI 7-10 item
				MP stage
1	C -> MP	27	EN	un-stuff Q10,Q11,Q12,H78,H79,H85,H347,C112,C129,C141,stuff H73,H89,P3 for drop EP000 function
2	C -> MP	31,32,33,35 36	PWR	change to short P/P:PL4,PL6,PL8,PL9,PL10,PL16,PL18,PL148,PL149,PL161,PL168 for C/D
3	C -> MP	35	EN	stuff PC51 for 1.05V_VDDST power
4	C -> MP	20	EN	change U29 to P8R201A & R107 to 4.7K for C/D